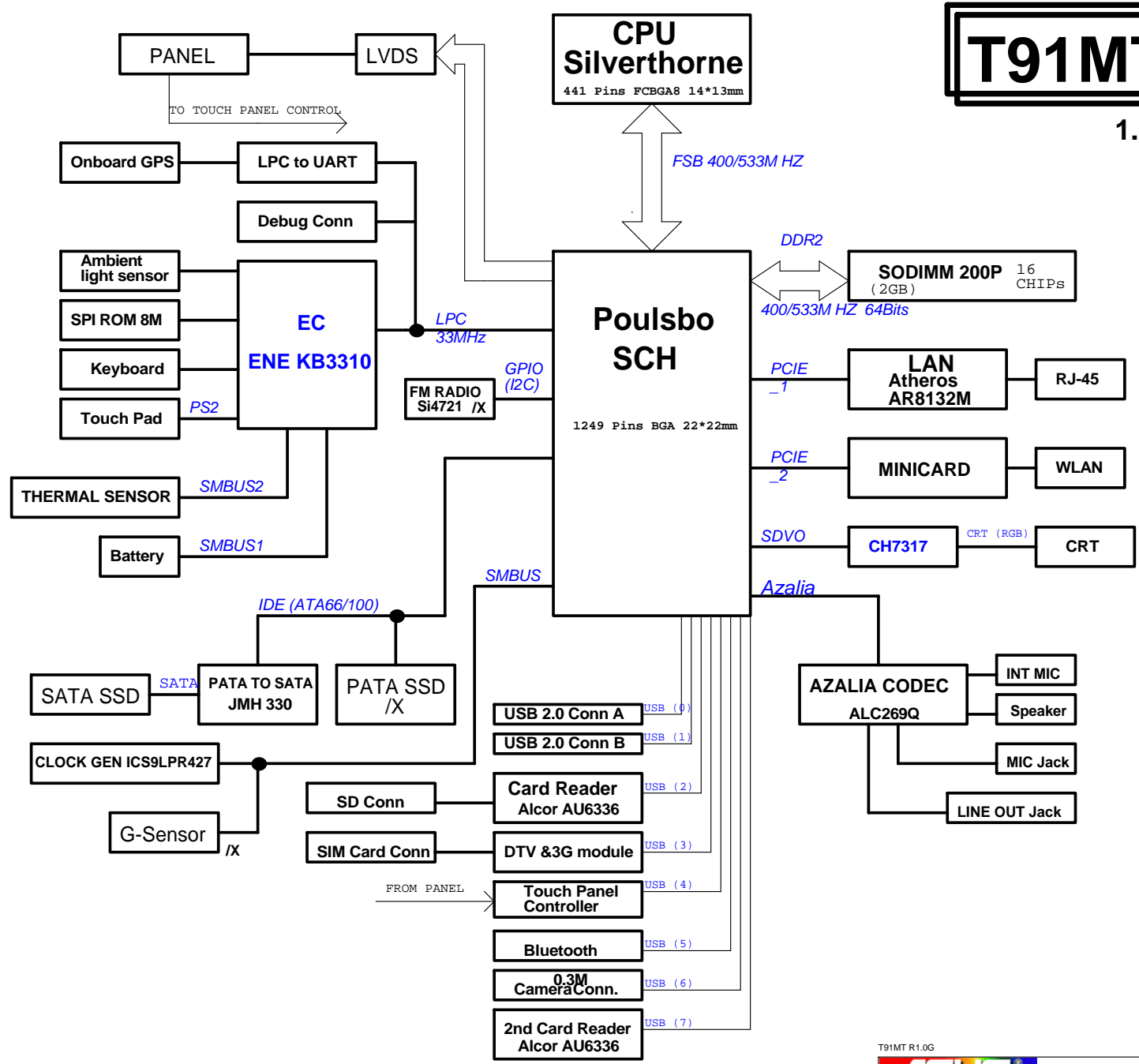


- 01_BLOCK DIAGRAM
- 02_SCH GPIO Setting
- 03_EC Pin Define
- 04_Power Sequrnse DC
- 05_Power Sequence AC
- 06_Power Sequence Description
- 07_Clock Gen_ICS9LPR427
- 08_CPU-SILVERTHORNE (1)
- 09_CPU-SILVERTHORNE (2)
- 10_CPU-SILVERTHORNE (3)
- 11_SCH_Poulsbo_HOST (1)
- 12_SCH_Poulsbo_DDR2 (2)
- 13_SCH_Poulsbo_LVDS/SDVO (3)
- 14_SCH_Poulsbo_PM/USB/IDE/AZ (4)
- 15_SCH_Poulsbo_STRAP(5)
- 16_SCH_Poulsbo_POWER (6)
- 17_SCH_Poulsbo_GND (7)
- 18_DDR2_SODIMM
- 19_DDR2_Termination
- 20_CH7317_SDVO_CRT
- 21_Onboard VGA
- 22_LCD Conn_LID
- 23_PCIEEx 3.5G & Ext. Antenna
- 24_Mini WIFI / BT
- 25_Bluetooth_BT253
- 26_FM_RADIO_Si4721
- 27_Onboard GPS
- 28_LAN_Atheros AR8113/AR8132
- 29_RJ45
- 30_Flash Conn
- 31_PATA_TO_SATA
- 32_USB Port
- 33_Card Reader_AU6336C52
- 34_Camera Conn
- 35_Codec_ALC269
- 36_Audio Amp Jack
- 37_EC_ENE KB3310
- 38_EC_UART Contoller
- 39_SPI_ROM_Debug Conn
- 40_Reset Map
- 41_KB_Touch Pad
- 42_Thermal Sensor
- 43_Small_Board_Conn
- 44_G-Sensor
- 45_Discharge
- 46_PWR Jack
- 47_SCREW HOLE
- 48_EMI
- 49_Power Flow
- 50_Vcore
- 51_Power System
- 52_Power_+1.8V & VTDDR
- 53_Power_VCCP
- 54_Power_+1.5VS & +2.5VS
- 55_Power_Charger
- 56_Power_Load Switch
- 57_Power Latch



T91MT

1.0G

T91MT R1.0G

		Title : Block Diagram	
ASUSTeK COMPUTER INC		Engineer: Leon Sun	
Size	Project Name	Date	Rev
Custom	T91MT	Tuesday, July 07, 2009	1.0G
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SCH GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIOUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIOUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
N45	GPIOUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIOUS3/ USBCC	Test Point	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	PCB ID	I/O CMOS3.3	Core	OFF	OFF	Input
F34	GPIO2	GPS_EN	I/O CMOS3.3	Core	OFF	OFF	Output
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

T91MT R1.0G Change list

page	Change list
7	CLK GEN427A->427C
11	FSB reference voltage R37 1K->1.2K
25	BT enable pin,level shift for slove BT pulse,add R230 R232 Q2, BT P/N 04G590032023
28	LAN AR8113->AR8132M
32	USB over current IC U7 U8 enable pin +5V_USB-> SUSB_ON,add C493 C492 10U
36	ALC269 A5->A6
37	EC KBC3310,A0->C1,OC18 4.7U for C1 version, pin63 for ALS
43	HOTKEY SW pull high R202 /X, CON3 pin9 for ALS

T91MT R1.0G

		Title : SCH GPIO Setting	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
A3	T91MT		
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EC KB3310 GPIO SETTING


Pin	Pin Name	Signal Name	Type	Note
1	GPIO0/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO4	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	BUF_RST#	I	
14	GPIO7	HOTKEY_SW1#	I	Battery over temperature
15	GPIO08	EXT_SM#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	Reserved for GPIO extender
18	GPIO0C/ESB_DAT	NC	O	Reserved for GPIO extender
19	GPIO0D	LID_EC_R#	I	Internal pull high
20	GPIO0E/SC#	KBC_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	PS-ON	O	latch power
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A	I	ALS
64	GPI39/AD1	BAT_B	I	
65	GPIO3A/AD2	BAT_C	I	
66	GPIO3B/AD3	BAT_D	I	
68	GPO3C/DA0	CHG_EN#	O	battery charger enabled

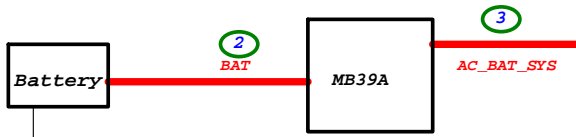
EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
122	XLCKI	K_XCLKI	I	
123	XLCKO	K_XCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

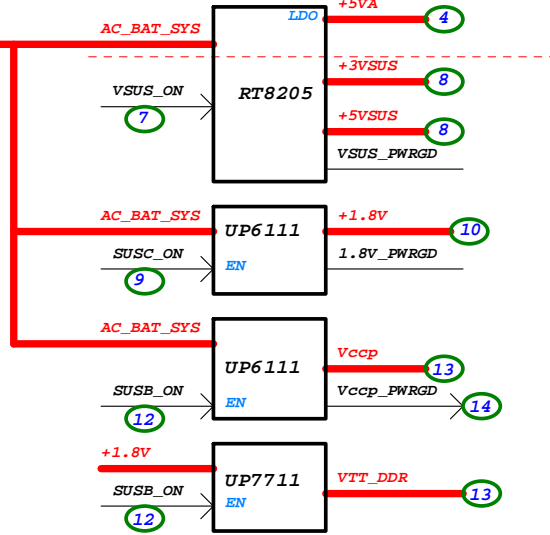
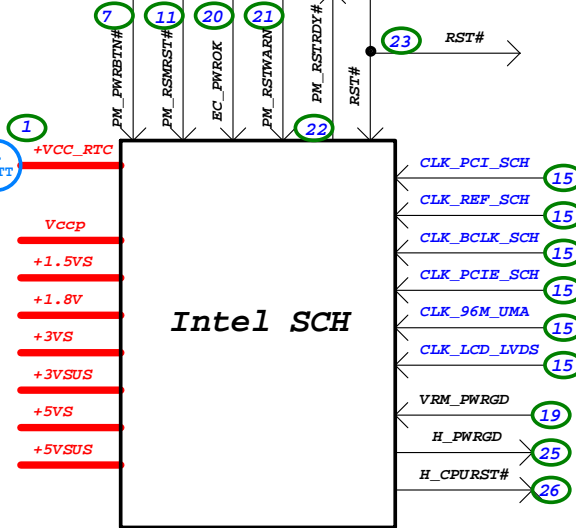
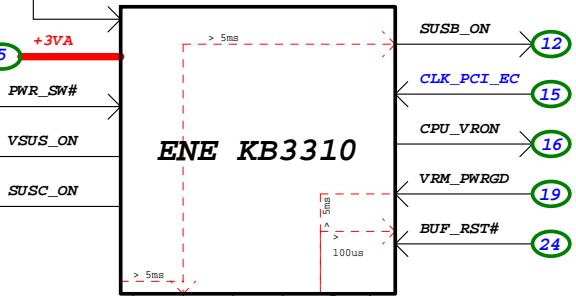
Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	Batt1 (Small/Internal): 1-present, 0-absent
76	GPI43	BAT2_IN	I	Batt2 (Small/Internal): 1-present, 0-absent
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB_ID0	I	for KB type detection
82	GPIO49/KSO17	KB_ID1	I	for KB type detection
83	GPIO4A/PSCLK1	N.C.	O	
84	GPIO4B/PSDAT1	N.C.	O	
85	GPIO4C/PSCLK2	N.C.	O	
86	GPIO4D/PSDAT2	GS2_INT2	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_UP#	O	Orange charger LED
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED#	O	
95	GPIO56	GS1_INT1	I	Internal pull high
97	GPXOA00/SDICS#	SPI_WP#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#	O	batt1 (Big/External) charging enabled. Batt1 is discharging priority in AC mode.
103	GPXOA06	CNT1_DIS#	O	batt1 discharging enabled
104	GPXOA07	CNT2_CHG#	O	batt2 (Small/Internal) charging enabled. Batt2 is charging priority in AC mode.
105	GPXOA08	CNT2_CHG#	O	batt2 discharging enabled
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	PM_PWROK	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	RST#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SLPRDY#	I	SLPRDY#, 100K pull down to GND
115	GPXID4	SLPMODE	I	SUSC#, 100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	PM_RSTRDY#	I	
118	GPXID7	RSTWARN	O	
121	GPIO57	GS1_INT2	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	GS2_INT1	O	

T91MT R1.0G

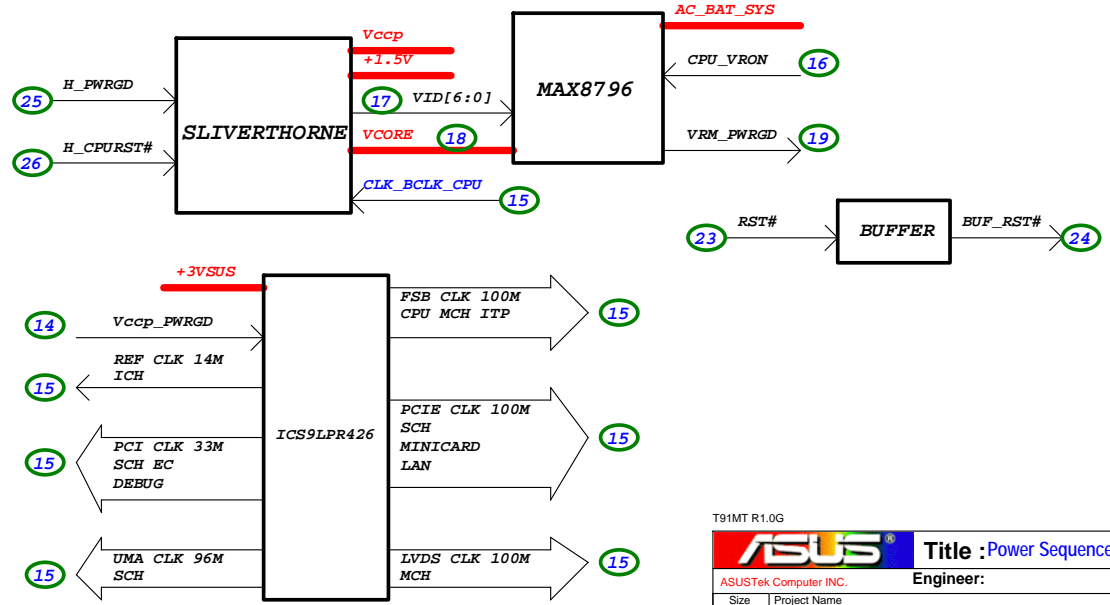
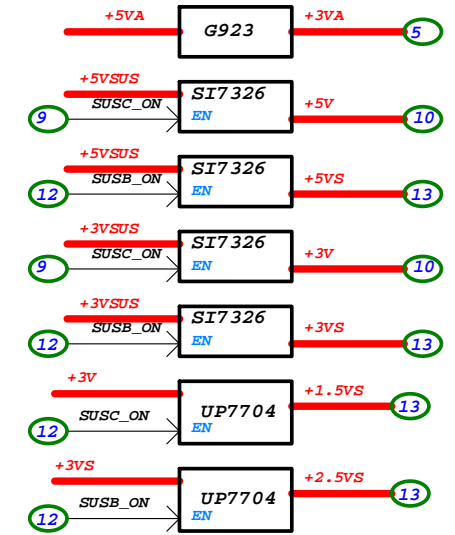
		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer:	
Size A3	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009	Sheet 3 of 57		



Signal	S0/S1	S3	S4/S5	Power
VSUS_ON	H	H	Adapter	H
			Battery	L
SUSB_ON	H	L	L	Main
SUSC_ON	H	H	L	DUAL



	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5VS	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	--	--	--	--	--	--	--	--	--	--	--



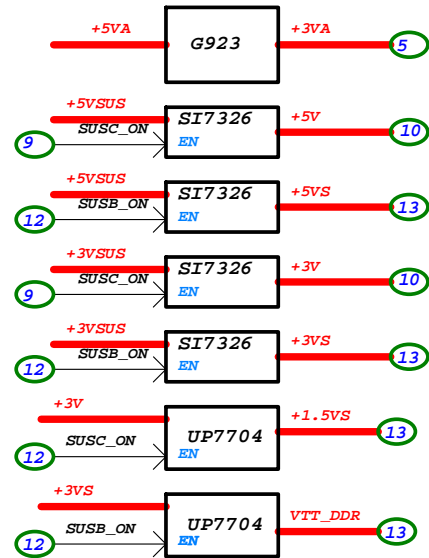
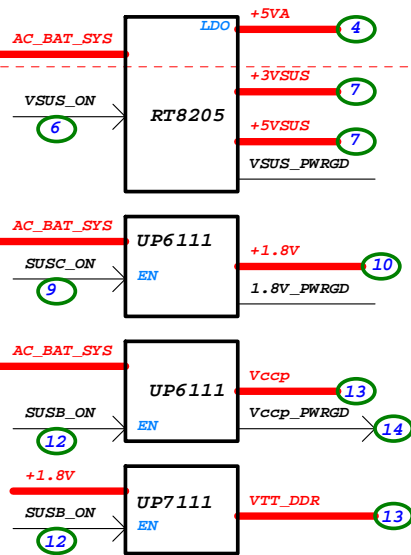
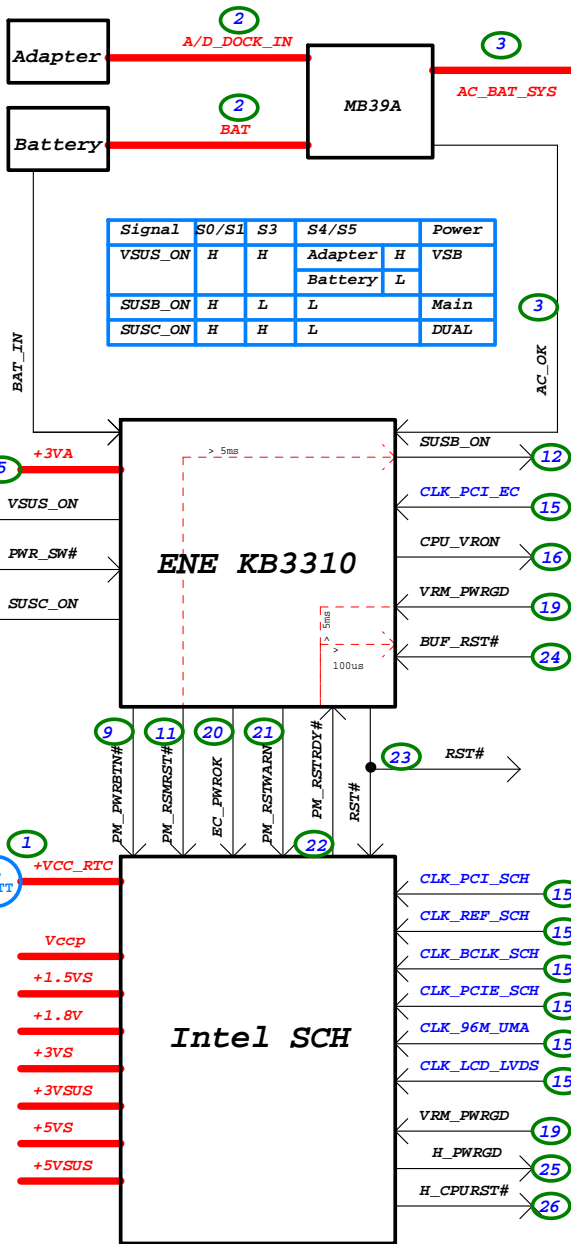
T91MT R1.0G

ASUS Title : Power Sequence DC

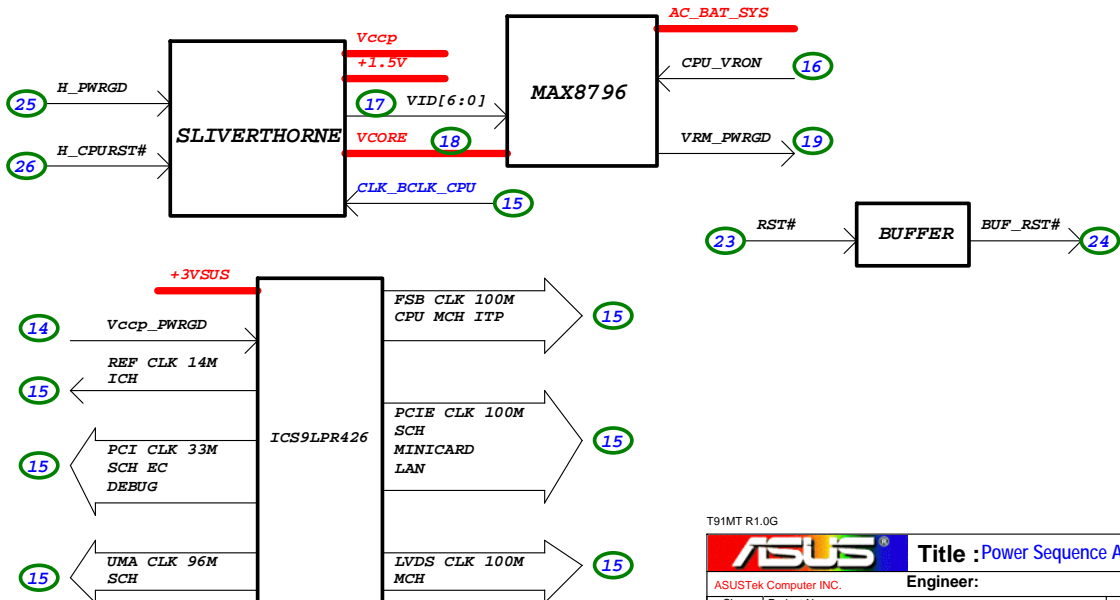
ASUSTek Computer INC. Engineer:

Size: A3 Project Name: T91MT Rev:

Date: Tuesday, July 07, 2009 Sheet 4 of 57



	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5VS	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	V	V	--	--	--	--	--	--	--	--	--



T91MT R1.0G

ASUS Title : Power Sequence AC

ASUS Computer INC. Engineer:

Size	Project Name	Rev
A3	T91MT	

Date: Tuesday, July 07, 2009 Sheet 6 of 57

S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for AC_OK until adaptor power is good, then
- 2.At least 5ms after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.
- 3.At least 20ms after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)
- 4.EC asserts RSTWARN.
- 5.SUSC_ON is asserted at least 20ms (de-bounce) after receiving PWR_SW#.
- 6.PM_RSMRST# is deasserted at least 5ms after SUSC power is stable.
- 7.At least 5ms after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 8.CPU_VRON is deasserted at least 100ms after SUSB power is stable.
- 9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 10.At least 10ms after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 11.Waiting for RSTRDY# until deasserted by SCH.
- 12.RESET# can be deasserted at lease 100us after PM_PWROK is asserted.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

- 1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.
- 2.For external wake event (PWR_SW#, keyboard wake up), then
- 3.EC asserts PM_PWRBTN# at least 50ms to wake SCH, and waiting for SLPRDY# until SCH deasserted.
- 4.EC asserts SUSB_ON to enable SUSB power.
- 5.CPU_VRON is deasserted at least 100ms after SUSB power is stable.
- 6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 7.At least 5ms after receiving CPUPWR_GD, ICH_PWROK is asserted.
- 8.Deasserts RSTWARN after ICH_PWROK is asserted.
- 9.RESET# can be deasserted 100us after RSTWARN is deasserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for BAT_IN until battery power is good, then
- 2.Waiting for PWR_SW# until user is pressed.
- 3.EC asserts VSUS_ON to enable VSUS power.
- 4.At least 20ms after VSUS power is stable.
- 5.EC asserts RSTWARN.
- 6.SUSC_ON is asserted at least 20ms (de-bounce) after receiving PWR_SW#.
- 7.PM_RSMRST# is deasserted at least 5ms after SUSC power is stable.
- 8.At least 5ms after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 9.CPU_VRON is deasserted at least 10ms after SUSB power is stable.
- 10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 11.At least 10ms after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 12.Waiting for RSTRDY# until deasserted by SCH.
- 13.RESET# can be deasserted at lease 100us after ICH_PWROK is asserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# for 1200ms to SCH after asserts RSTWARN.
- 4.EC deasserts RSTWARN.
- 5.EC deasserts RESET# after at least 100us delay from RSTWARN.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

- 1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).
- 2.At least 20ms after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50ms width) to SCH.
- 3.Waiting for SLPRDY# until has been asserted.
- 4.EC asserts RSTWARN to SCH to begin internal sequence.
- 5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.
- 6.EC asserts RESET# after detecting RSTRDY# asserted.
- 7.EC deasserts ICH_PWROK.
- 8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

- 9.EC asserts PM_RSMRST#.
- 10.EC deasserts SUSC_ON to turn off the other power planes.
- 11.EC deasserts VSUS_ON if in battery mode.
- 12.EC deasserts RSTWARN to save more power.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

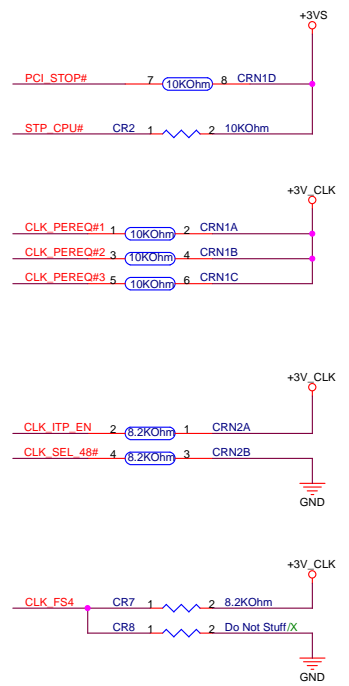
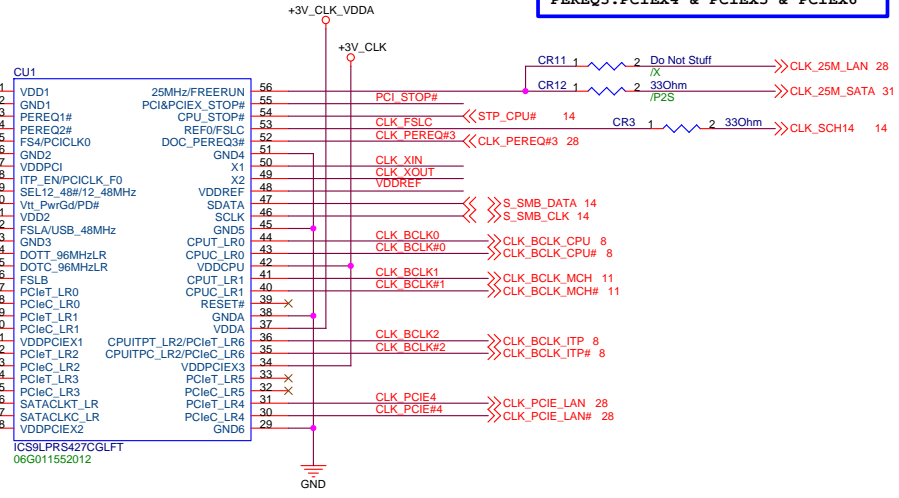
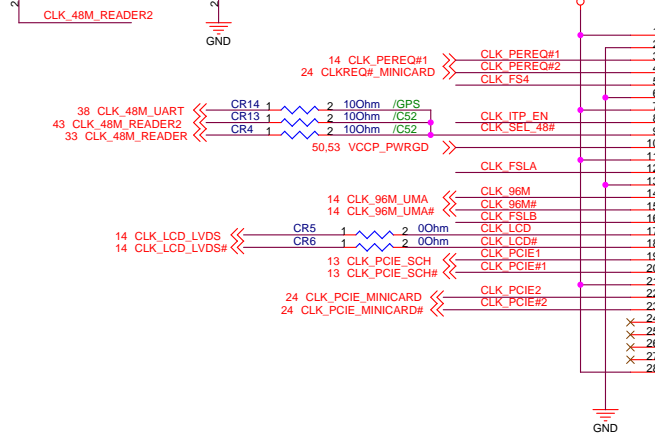
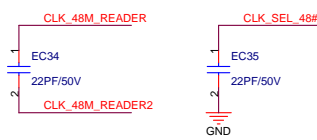
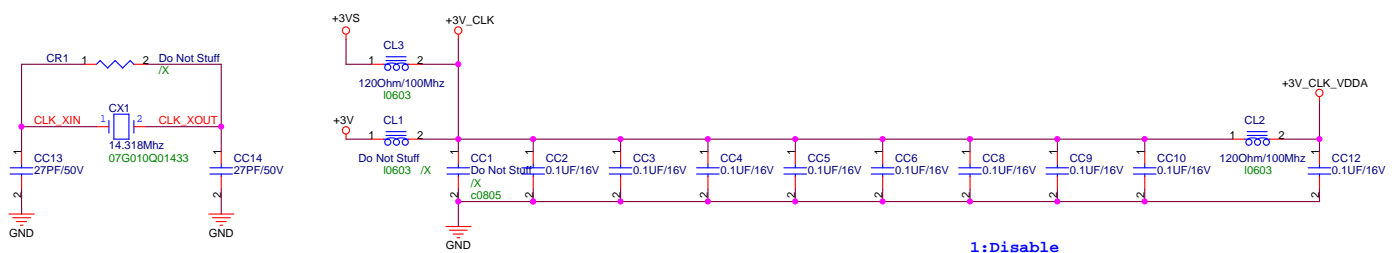
Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# to SCH after asserts RSTWARN.
- 4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.
- 5.EC asserts PM_RSMRST# after CPU_VRON power is off.
- 6.EC disables SUSC_ON power for 3-5 seconds.
- 7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.

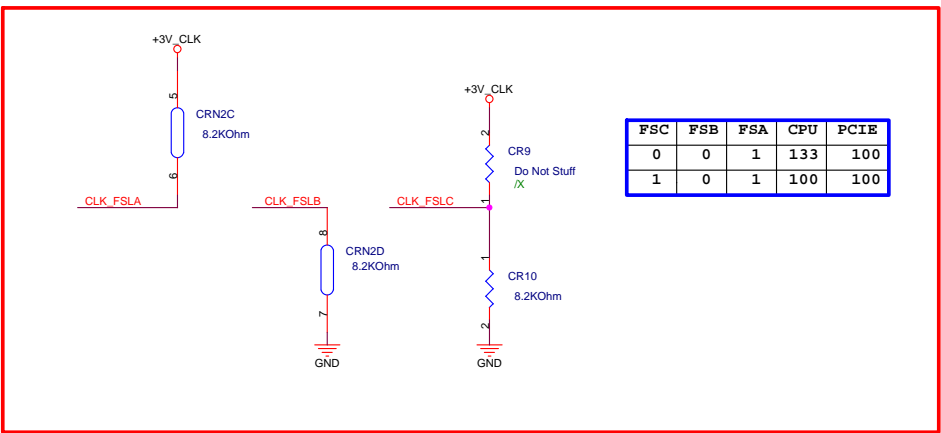
T91MT R1.0G

Power Sequence Description

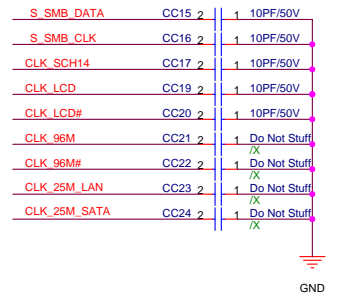
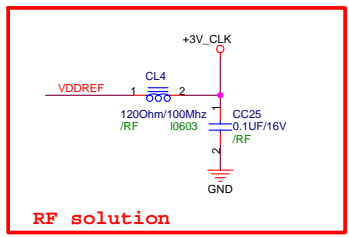
		Title :	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	T91MT		
Date: Tuesday, July 07, 2009		Sheet	6 of 57



427CGLFT: 06G011552012 (Default)
427AGLF: 06G011552010



FSC	FSB	FSA	CPU	PCIE
0	0	1	133	100
1	0	1	100	100



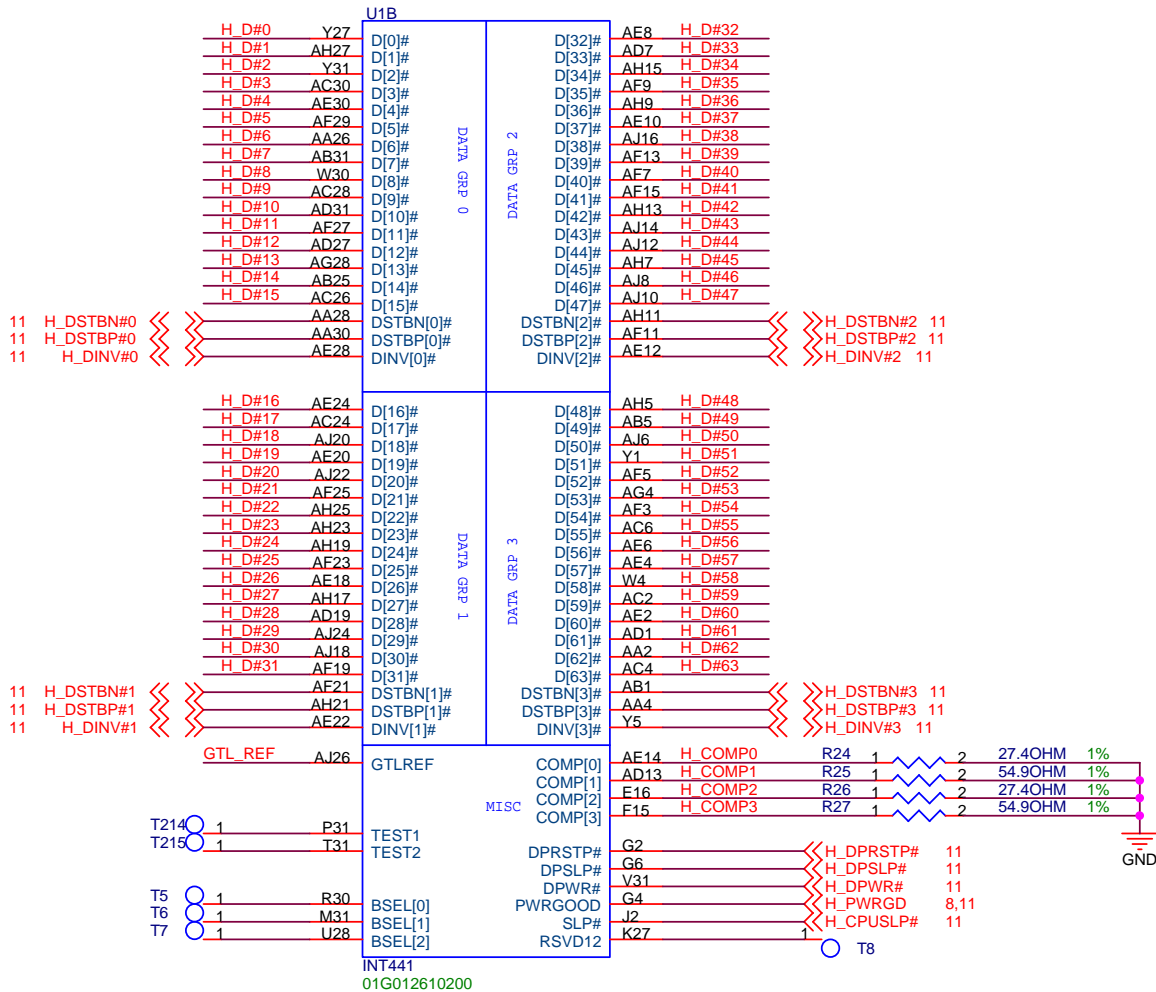
T91MT R.1.0G

ASUS Title : Clock Gen_IC9S9LPRS427

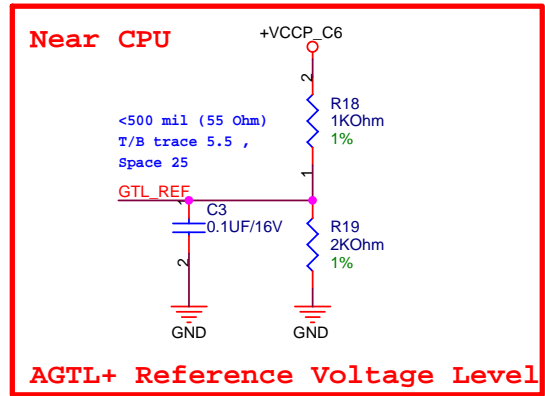
ASUSTek Computer INC. Engineer:

Size	Project Name	Rev
A3	T91MT	

Date: Tuesday, July 07, 2009 Sheet 7 of 57



H_D#63:0 <<>> H_D#63:0] 11



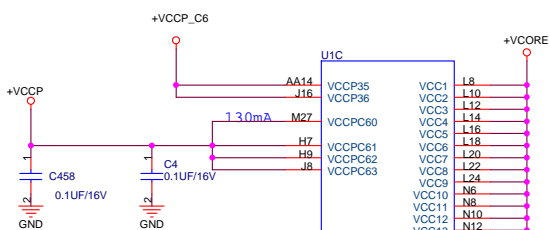
Layout Note

COMP 0 2 connect with Z0=27.4 ohm, L<0.5"

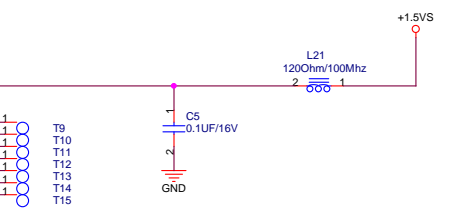
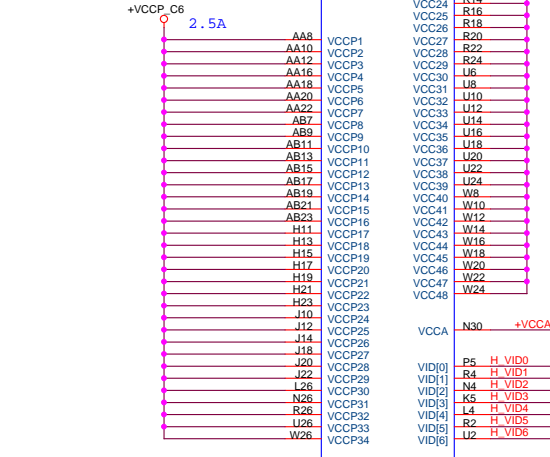
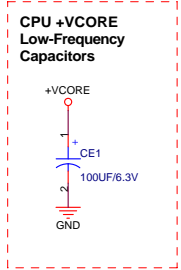
COMP 1 3 connect with Z0=55 ohm, L<0.5"

T91MT R1.0G

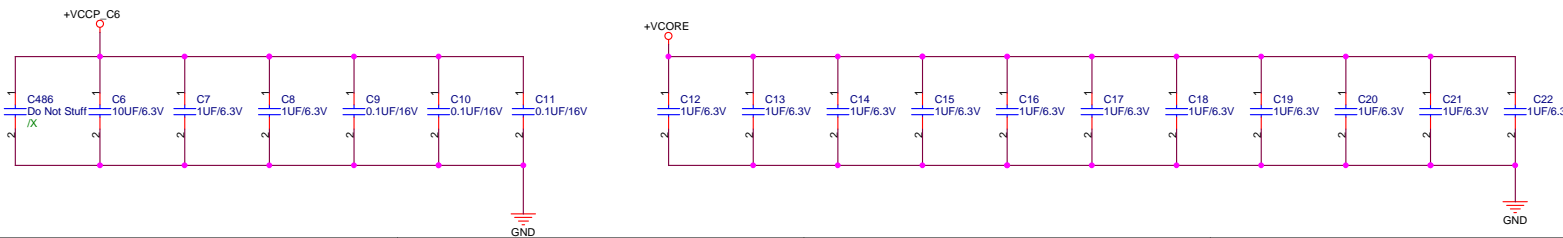
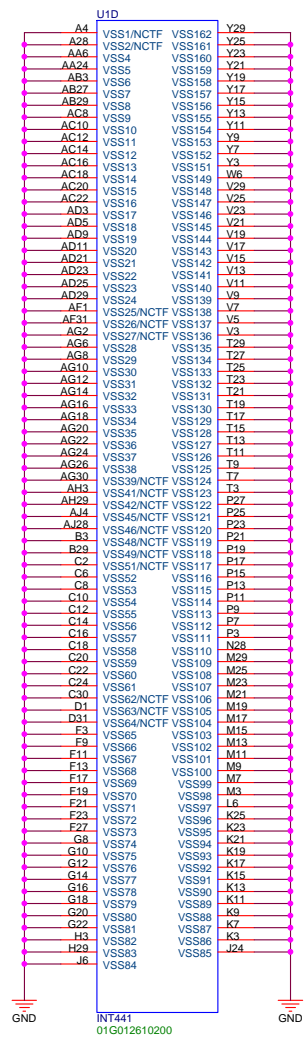
ASUS		Title : CPU-SLIVERTHORNE(1)	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009		Sheet	9 of 57



CPU TYPE	Vcore	Freq
Silverthorne Standard Voltage	0.98V @HFM TBD @LFM	TBD
Processilverthorne Medium Voltage	0.8V @HFM TBD @LFM	TBD
Processilverthorne Low Voltage	0.76V @HFM TBD @LFM	TBD



Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 18mil trace, 7mil vccsense to vssense spacing. 25 mil spacing from others. Place PU and PD within 1 inch of CPU.



T91MT R.1.0G

ASUS Title :CPU-SILVERTHORNE (2)

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	T91MT	

Date: Tuesday, July 07, 2009 Sheet 10 of 57

18 MA_DQ[63:0] <<>

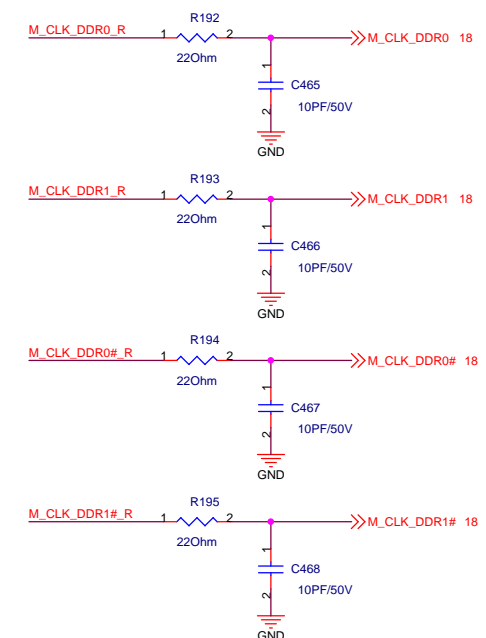
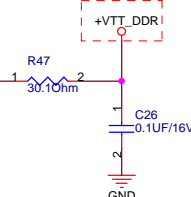
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MA_DQ1	BG47	SM_DQ1
MA_DQ2	BE45	SM_DQ2
MA_DQ3	BC43	SM_DQ3
MA_DQ4	BE42	SM_DQ4
MA_DQ5	BC47	SM_DQ5
MA_DQ6	BC45	SM_DQ6
MA_DQ7	BK44	SM_DQ7
MA_DQ8	BK42	SM_DQ8
MA_DQ9	BK40	SM_DQ9
MA_DQ10	BC41	SM_DQ10
MA_DQ11	BC41	SM_DQ11
MA_DQ12	BG43	SM_DQ12
MA_DQ13	BJ43	SM_DQ13
MA_DQ14	BJ39	SM_DQ14
MA_DQ15	BC39	SM_DQ15
MA_DQ16	BC39	SM_DQ16
MA_DQ17	BK38	SM_DQ17
MA_DQ18	BG37	SM_DQ18
MA_DQ19	BK36	SM_DQ19
MA_DQ20	BJ37	SM_DQ20
MA_DQ21	BG35	SM_DQ21
MA_DQ22	BJ35	SM_DQ22
MA_DQ23	BC35	SM_DQ23
MA_DQ24	BK34	SM_DQ24
MA_DQ25	BG31	SM_DQ25
MA_DQ26	BG33	SM_DQ26
MA_DQ27	BK30	SM_DQ27
MA_DQ28	BC33	SM_DQ28
MA_DQ29	BJ33	SM_DQ29
MA_DQ30	BJ31	SM_DQ30
MA_DQ31	BC31	SM_DQ31
MA_DQ32	BJ29	SM_DQ32
MA_DQ33	BC29	SM_DQ33
MA_DQ34	BK28	SM_DQ34
MA_DQ35	BC29	SM_DQ35
MA_DQ36	BE27	SM_DQ36
MA_DQ37	BK26	SM_DQ37
MA_DQ38	BG25	SM_DQ38
MA_DQ39	BJ25	SM_DQ39
MA_DQ40	BC25	SM_DQ40
MA_DQ41	BG23	SM_DQ41
MA_DQ42	BK22	SM_DQ42
MA_DQ43	BJ21	SM_DQ43
MA_DQ44	BK24	SM_DQ44
MA_DQ45	BJ23	SM_DQ45
MA_DQ46	BC21	SM_DQ46
MA_DQ47	BC21	SM_DQ47
MA_DQ48	BK20	SM_DQ48
MA_DQ49	BJ19	SM_DQ49
MA_DQ50	BG17	SM_DQ50
MA_DQ51	BJ17	SM_DQ51
MA_DQ52	BC19	SM_DQ52
MA_DQ53	BC19	SM_DQ53
MA_DQ54	BC17	SM_DQ54
MA_DQ55	BK16	SM_DQ55
MA_DQ56	BG15	SM_DQ56
MA_DQ57	BC15	SM_DQ57
MA_DQ58	BJ13	SM_DQ58
MA_DQ59	BK12	SM_DQ59
MA_DQ60	BK14	SM_DQ60
MA_DQ61	BJ15	SM_DQ61
MA_DQ62	BC13	SM_DQ62
MA_DQ63	BC11	SM_DQ63

U2D

DDR SYSTEM MEMORY

SM_BS0	BC27	MA_BA0
SM_BS1	BE25	MA_BA1
SM_BS2	BA35	MA_BA2
SM_CK0	BG45	M_CLK_DDR0_R
SM_CK1	BE11	M_CLK_DDR1_R
SM_CK0#	BJ45	M_CLK_DDR0#_R
SM_CK1#	BG11	M_CLK_DDR1#_R
SM_CKE0	BE39	MA_CKE0 18,19
SM_CKE1	BE37	MA_CKE1 18,19
SM_DQS0	BJ47	MA_DQS0
SM_DQS1	BJ41	MA_DQS1
SM_DQS2	BC37	MA_DQS2
SM_DQS3	BK32	MA_DQS3
SM_DQS4	BG27	MA_DQS4
SM_DQS5	BE23	MA_DQS5
SM_DQS6	BK18	MA_DQS6
SM_DQS7	BG13	MA_DQS7
SM_MA0	BJ27	MA_MA0
SM_MA1	BA19	MA_MA1
SM_MA2	BA27	MA_MA2
SM_MA3	BA25	MA_MA3
SM_MA4	BE29	MA_MA4
SM_MA5	BC23	MA_MA5
SM_MA6	BE31	MA_MA6
SM_MA7	BA31	MA_MA7
SM_MA8	BA33	MA_MA8
SM_MA9	BA29	MA_MA9
SM_MA10	BE17	MA_MA10
SM_MA11	BE35	MA_MA11
SM_MA12	BE33	MA_MA12
SM_MA13	BE19	MA_MA13
SM_MA14	BA37	MA_MA14
SM_VREF	BE43	DDR_VREF 18
SM_RAS#	BE21	MA_RAS# 18,19
SM_CAS#	BA13	MA_CAS# 18,19
SM_WE#	BA17	MA_WE# 18,19
SM_CS0#	BA23	MA_CS#0 18,19
SM_CS1#	BA15	MA_CS#1 18,19
SM_RCOMP0	BE13	SM_RCOMP0
SM_RCVENIN	BA39	MA_RCVENIN
SM_RCVENOUT	BE41	MA_RCVENOUT

Note: TOTAL LENGTH <1"



02G010018704

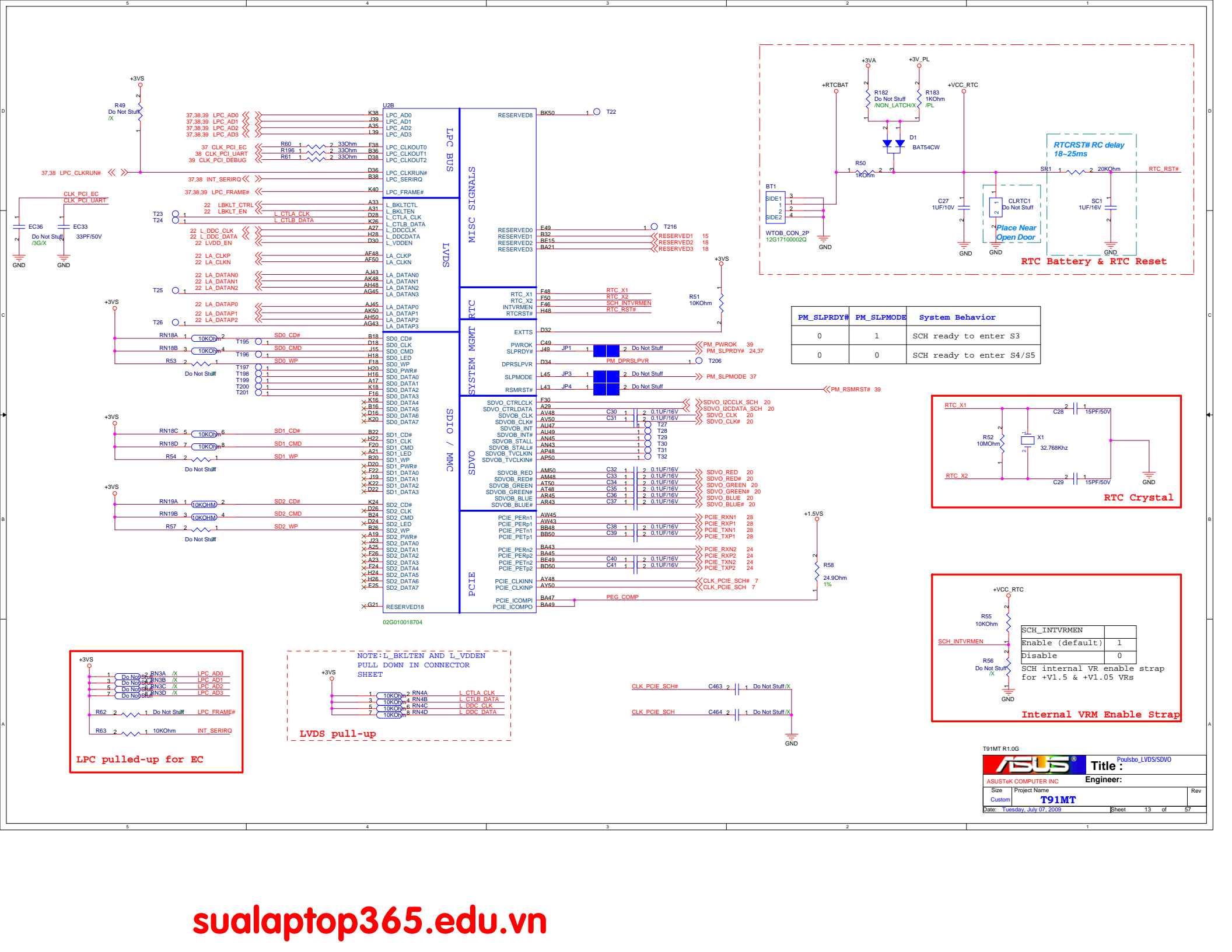
T91MT R1.0G

ASUS Title : Poulsbo_DDR2 (2)

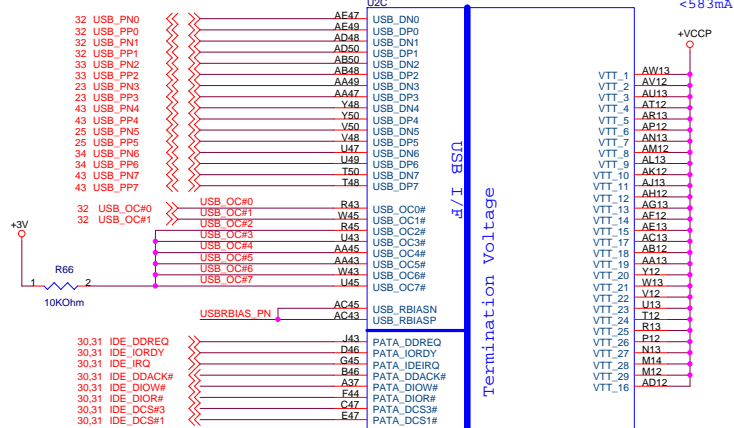
ASUSTek Computer INC. Engineer:

Size	Project Name	Rev
Custom	T91MT	

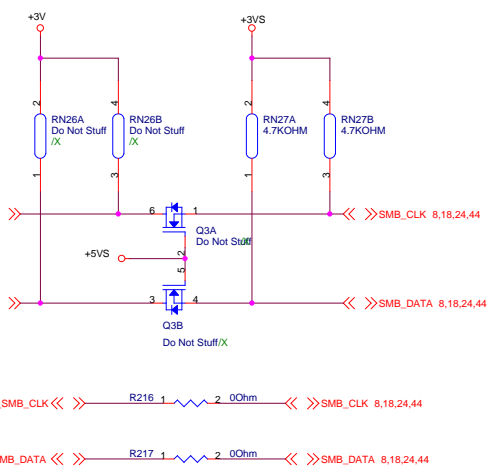
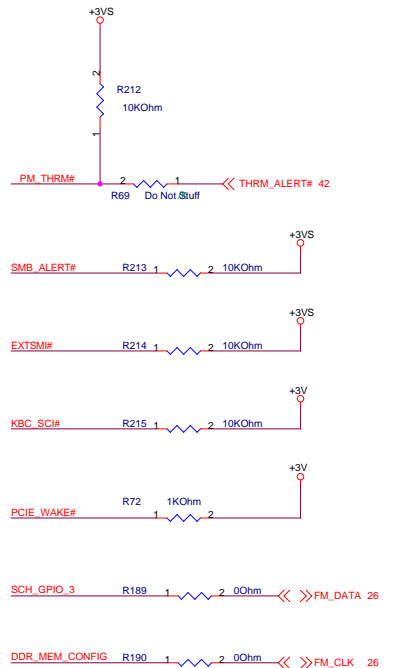
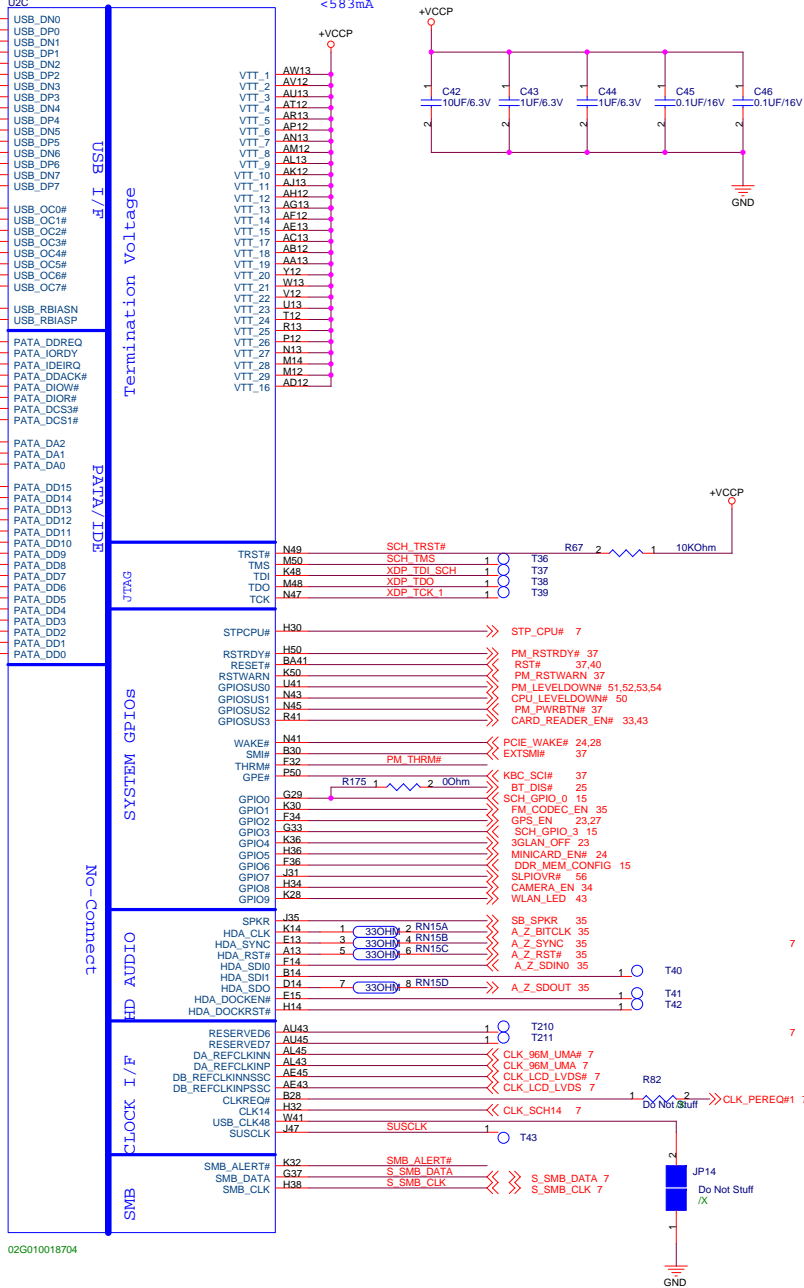
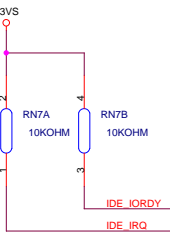
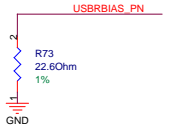
Date: Tuesday, July 07, 2009 Sheet 12 of 57



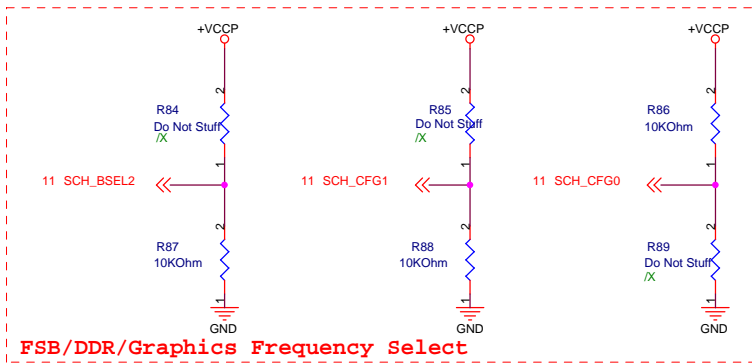
USB 0	USB PORT
USB 1	USB PORT
USB 2	Card Reader
USB 3	3.5G
USB 4	Touch Panel
USB 5	Bluetooth
USB 6	Camera
USB 7	2'nd Card Reader



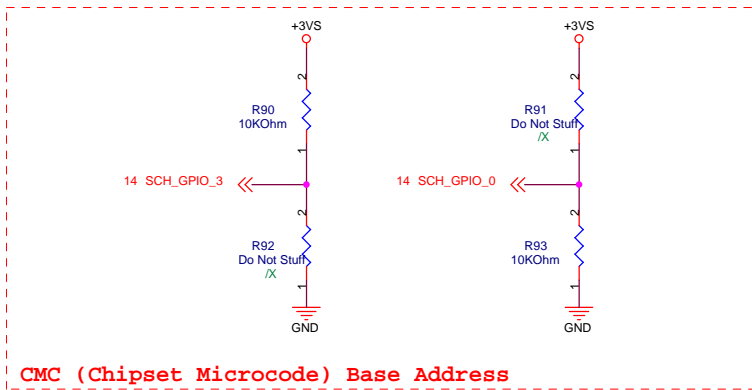
30.31 IDE_DD[15:0] << IDE_DD15[0]
 30.31 IDE_DA[2:0] << IDE_DA12[0]



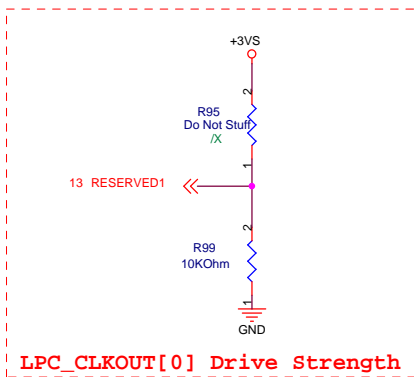
T91MT R1.0G
ASUS Title : SCH_Poulsbo_PMUSBIDEAZ(0)
 ASUSTek COMPUTER INC Engineer:
 Size Project Name Rev
 Custom T91MT
 Date: Tuesday, July 07, 2009 Sheet 14 of 57



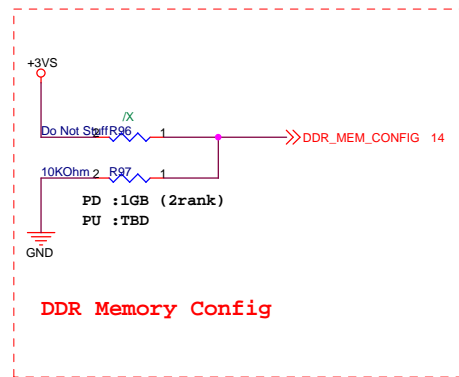
FSB/DDR/Graphics Frequency Select



CMC (Chipset Microcode) Base Address



LPC_CLKOUT[0] Drive Strength



DDR Memory Config

Strap Function	Signal Name			Strap		Comment
FSB/DDR Frequency Select Graphics Frequency Select	SCH_BSEL2	SCH_CFG1	SCH_CFG0	Gfx_Freq	FSB	Note: Clock Frequencies are in Mhz Default Frequency determined by FSB speed
	0	0	0	200	400	
	0	0	1	200	533	
CMC (Chipset Microcode) Base Address	GPIO3		GPIO0		Address	Selects the starting address that the CMC will use to start fetching code. (GPIO3 is the most significant)
	0	0		0xFFFFB0000		
	0	1		0xFFFFC0000		
	1	0		0xFFFFD0000 (default)		
	1	1		0xFFFFE0000		
LPC_CLKOUT[0] Buffer Strength	RESERVED1			Value		Selects the drive strength of the LPC_CLKOUT[0] clock.
	0			Reserved		
	0			1 Load (Default)		
	1			Reserved		
	1			2 Loads		

T91MT R1.0G

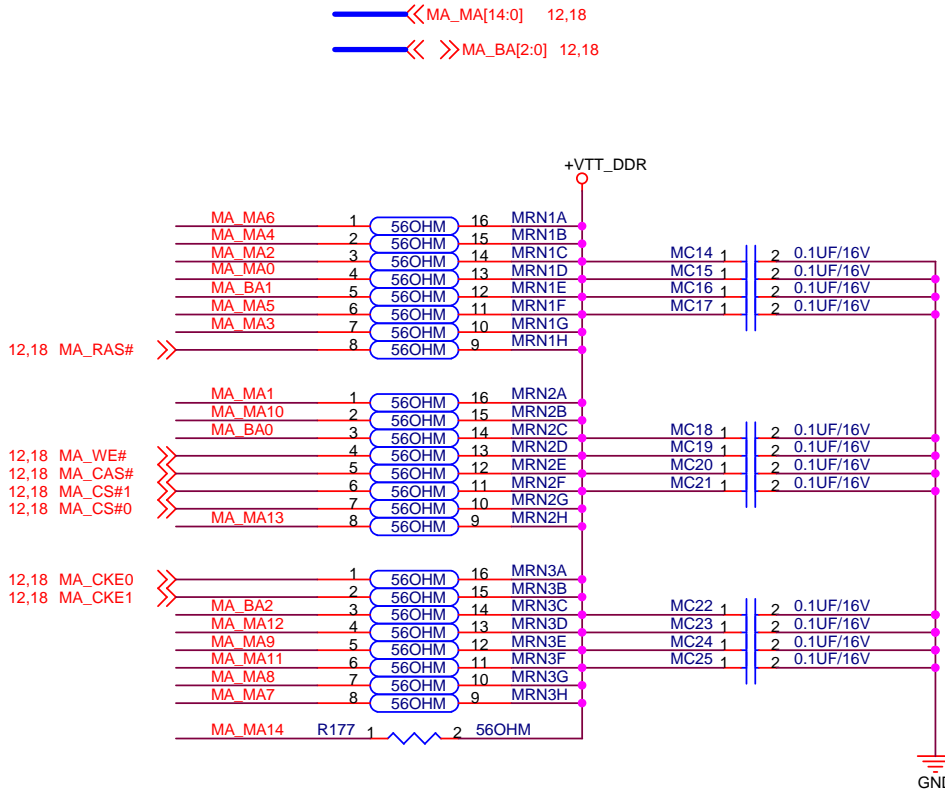


ASUSTek Computer INC. Engineer:

Size Project Name Rev

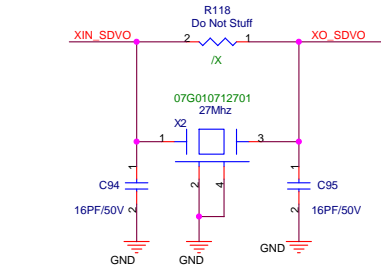
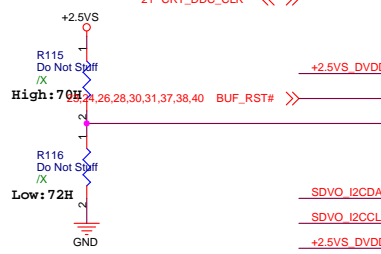
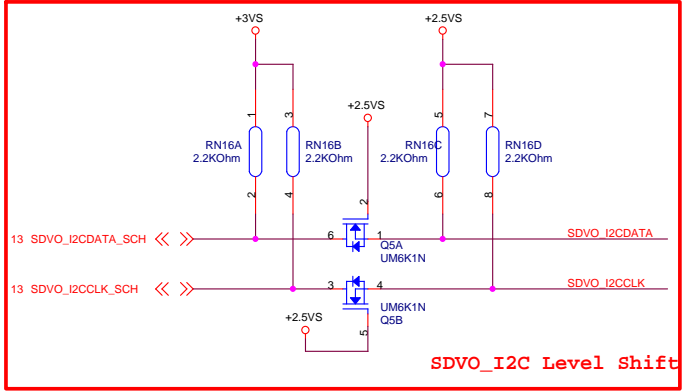
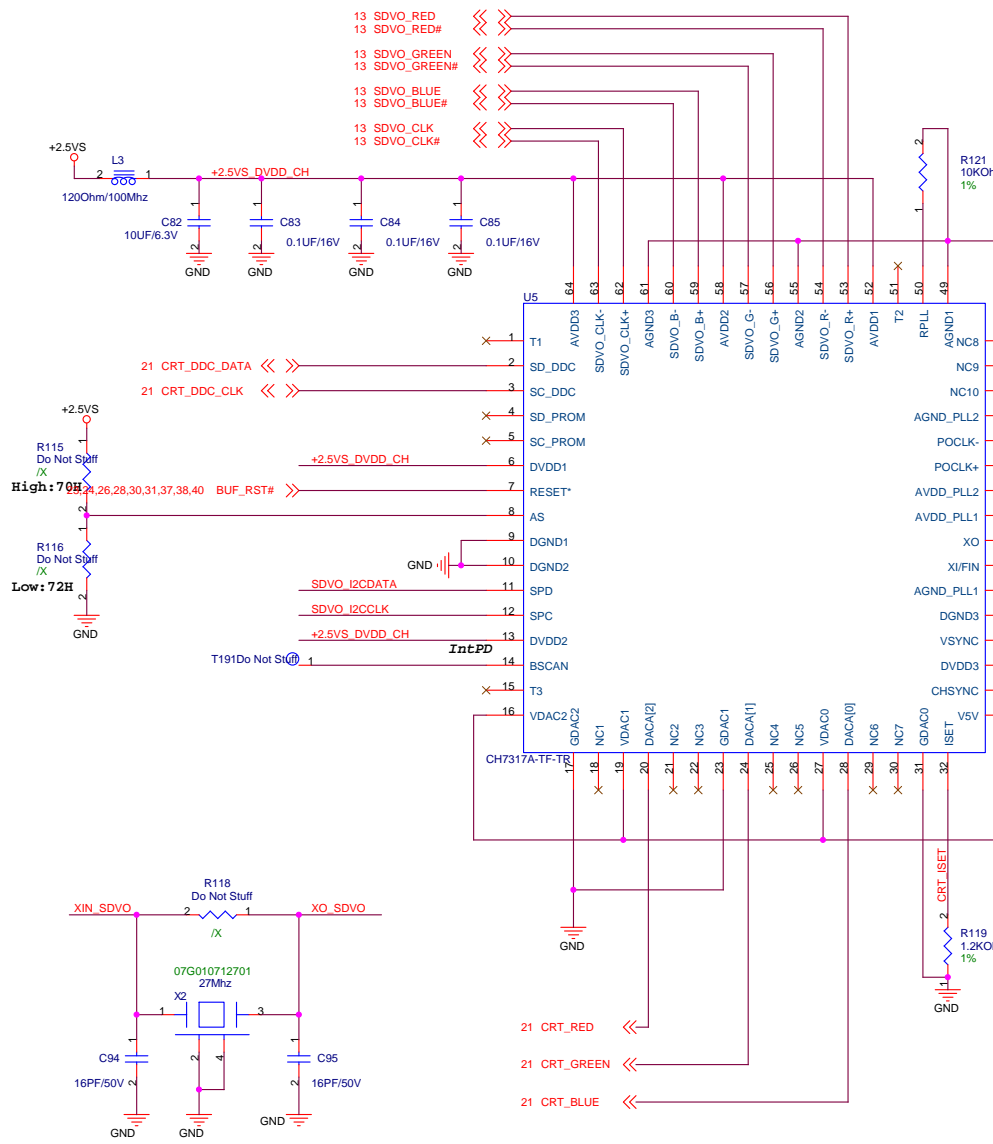
B T91MT

Date: Tuesday, July 07, 2009 Sheet 15 of 57



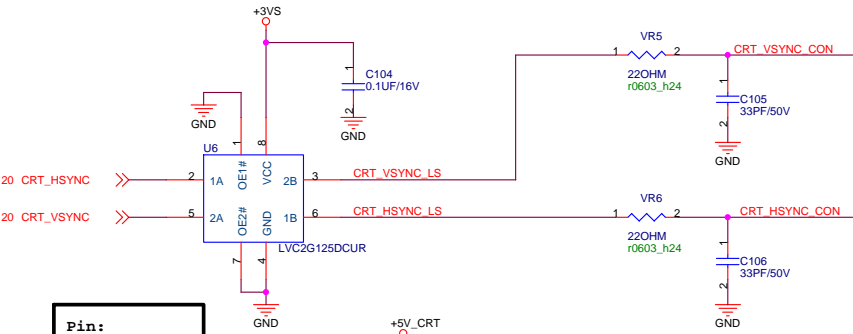
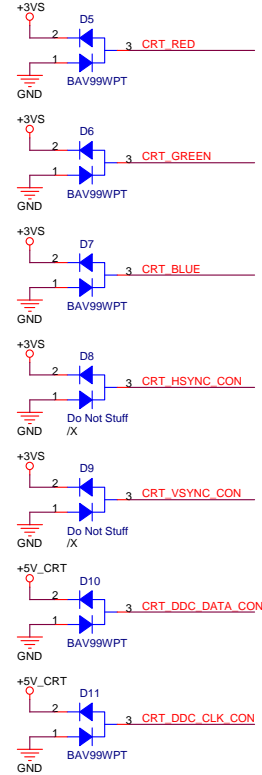
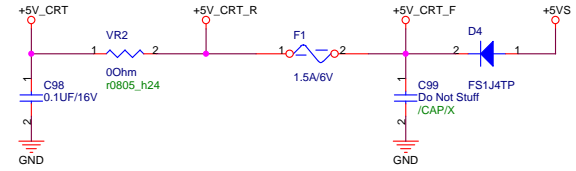
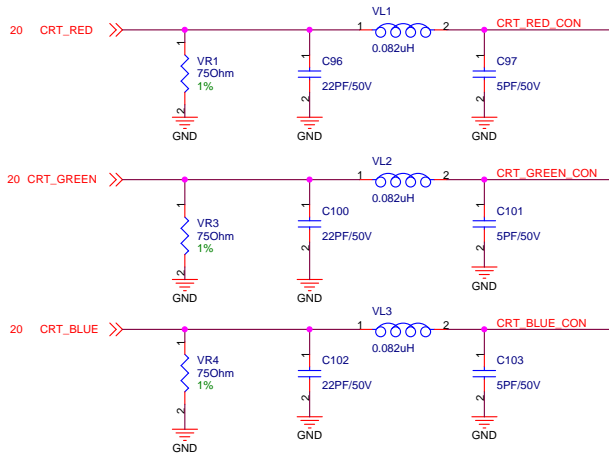
T91MT R1.0G

		Title : DDR2_Termination
ASUSTek Computer INC.		Engineer:
Size A4	Project Name T91MT	Rev
Date: Tuesday, July 07, 2009	Sheet 19 of 57	



XTAL Height 1mm

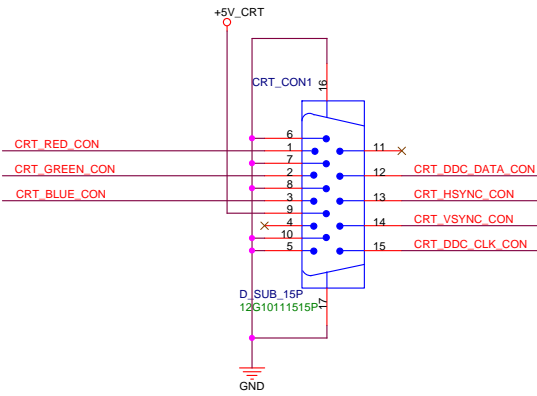
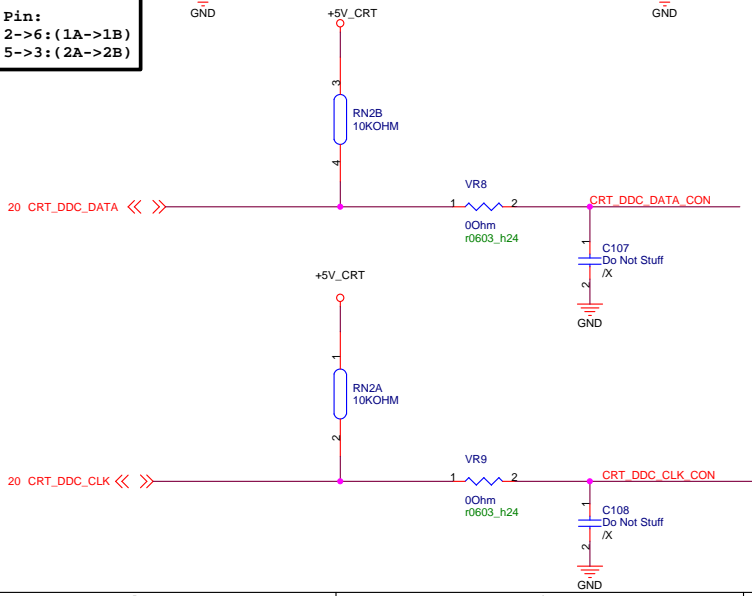
T91MT R1.0G		ASUS Title : CH7317_SDVO_CRT	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
A3	T91MT		
Date:	Tuesday, July 07, 2009	Sheet	20 of 57



C105 C106 for EA measurement
 U6_1:VR5 & VR6-->22 OHM
 U6 /X :VR5 & VR6 -->0 OHM

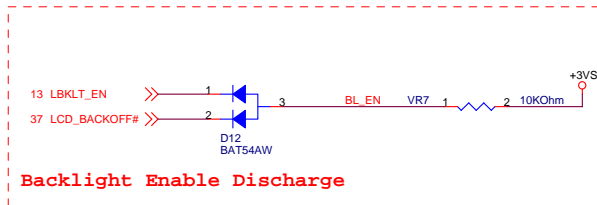
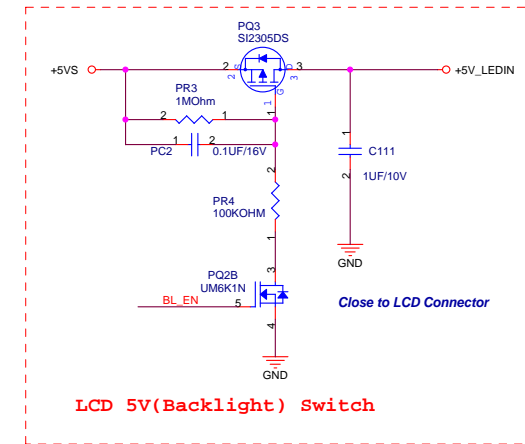
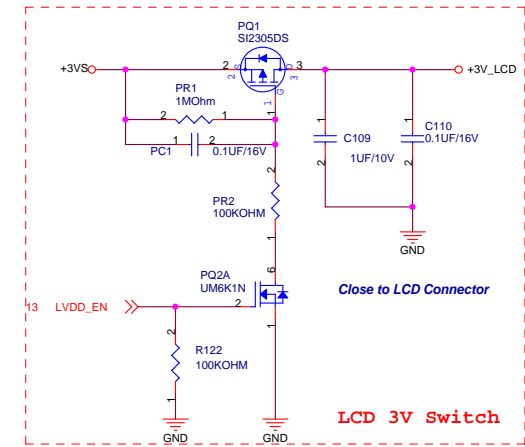
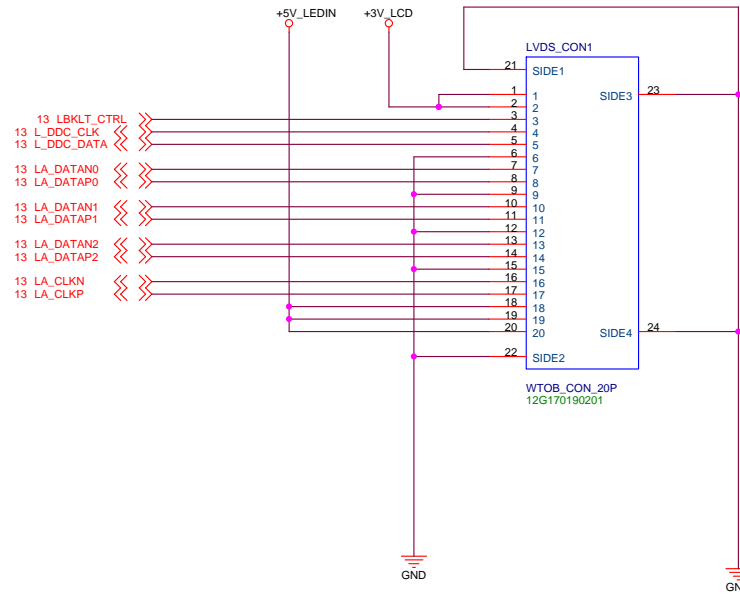
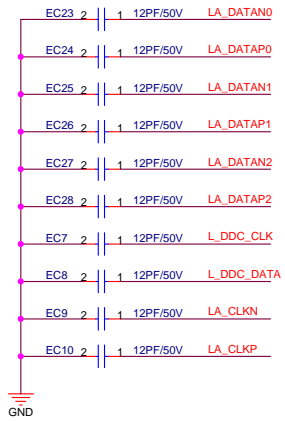
BUS BUFFER:
 Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

Pin:
 2->6: (1A->1B)
 5->3: (2A->2B)



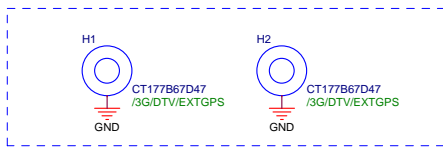
T91MT R1.0G

ASUS		Title : Onboard VGA	
ASUSTek Computer INC.		Engineer:	
Size A3	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009	Sheet 21	of 57	

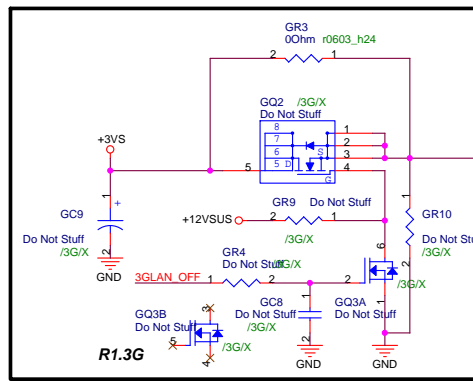


T91MT R1.0G

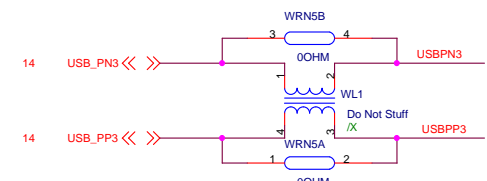
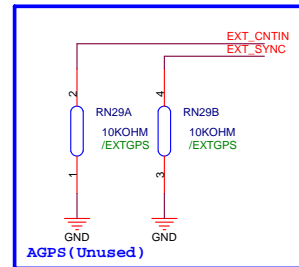
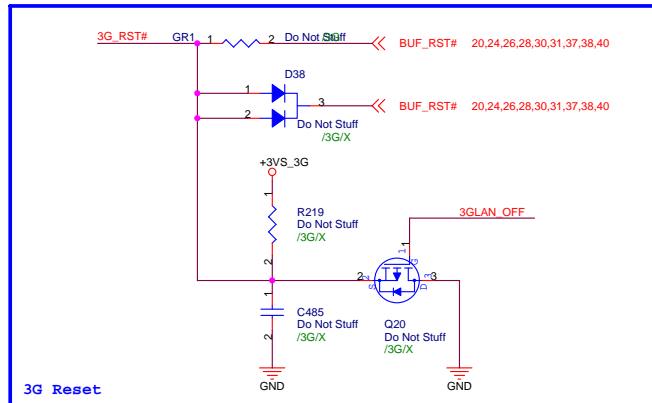
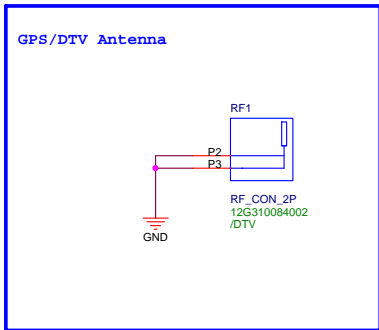
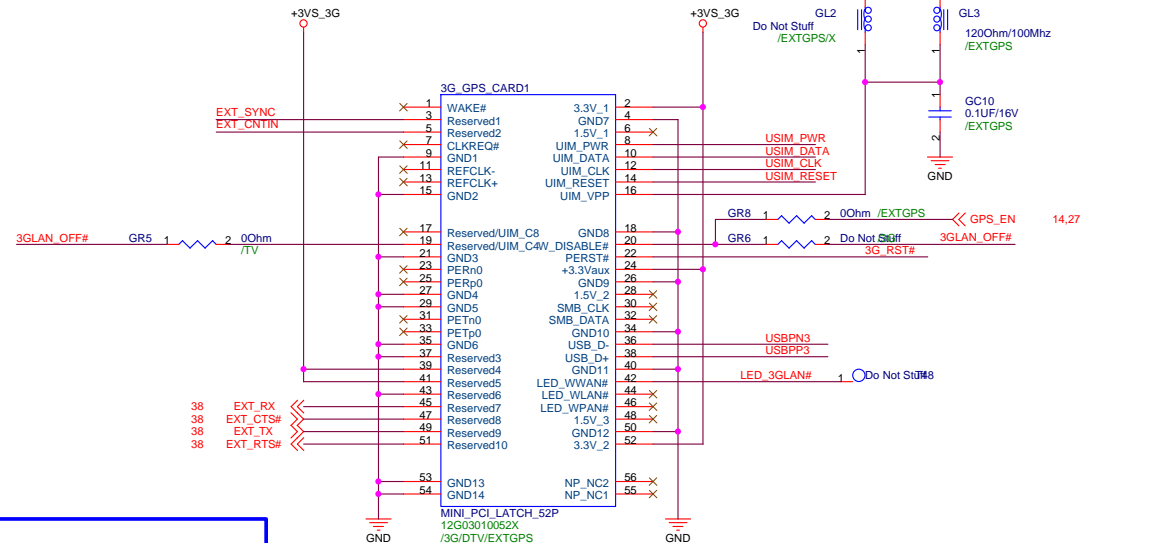
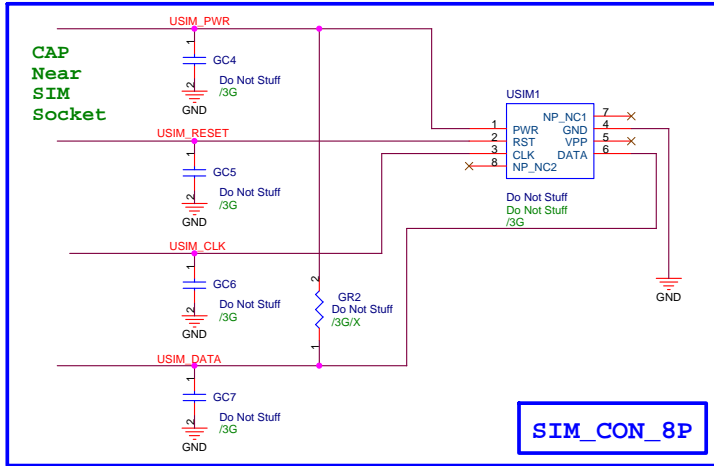
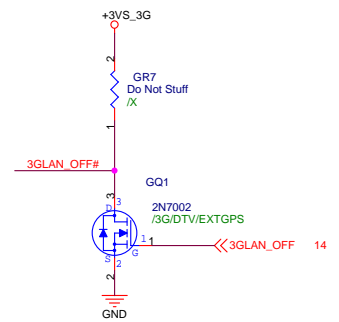
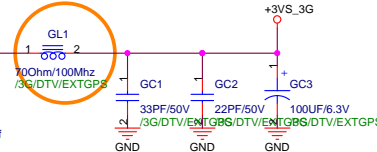
ASUS		Title : LVDS Conn	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
A3	T91MT		
Date: Tuesday, July 07, 2009		Sheet 22	of 57



MINI CARD NUT(2.8mm) *2

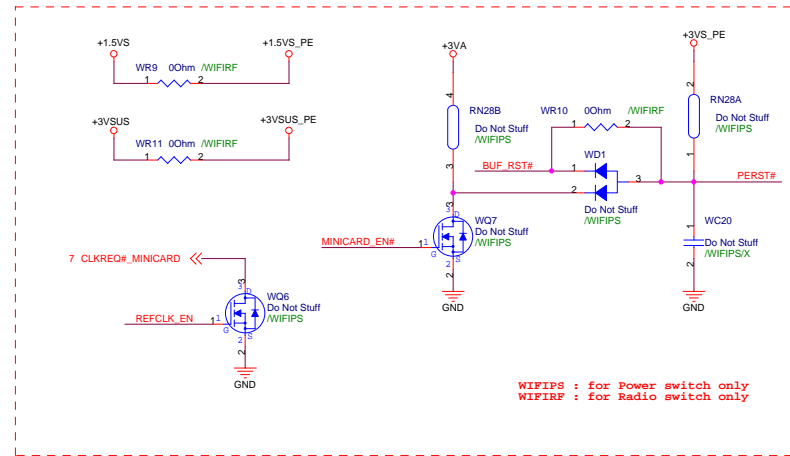
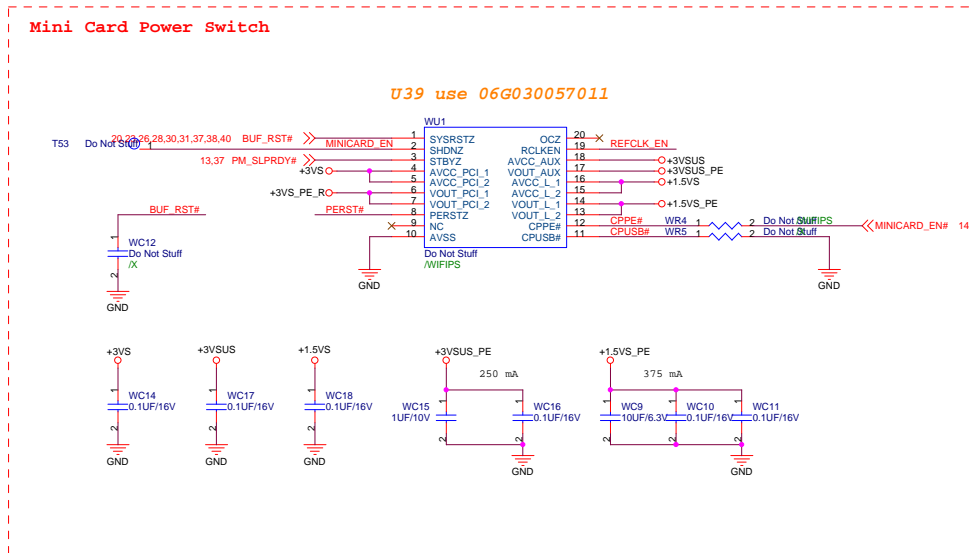
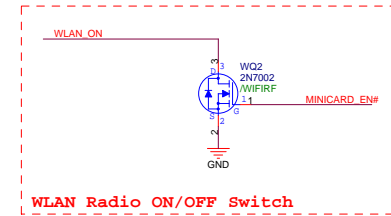
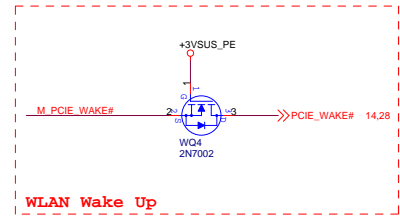
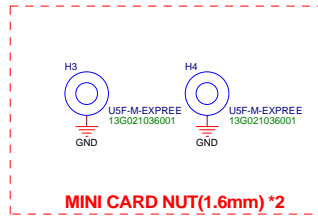
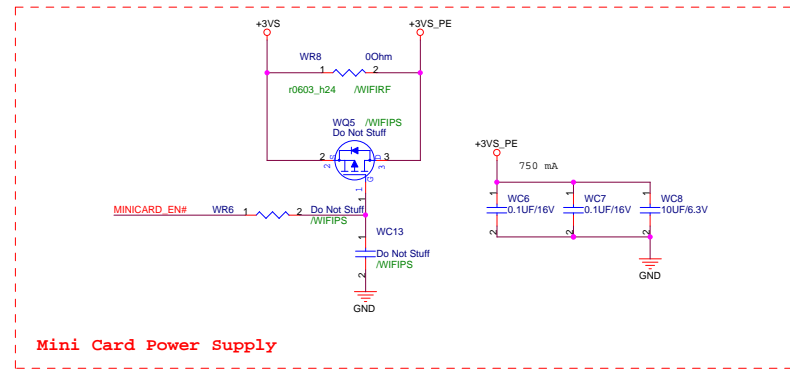
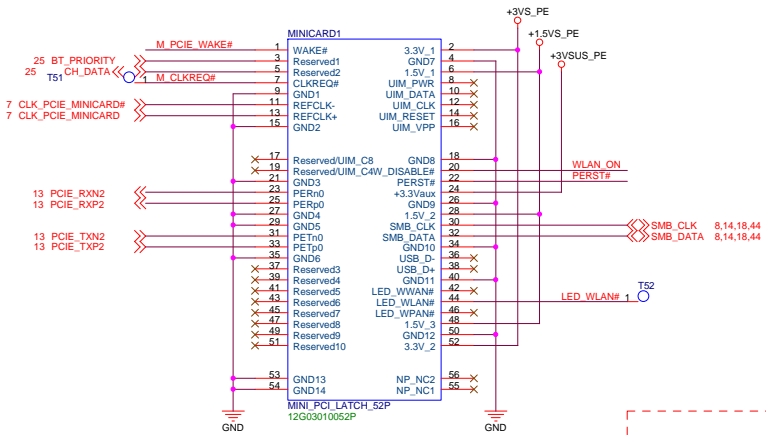


2008/03/11 change to high rated current bead



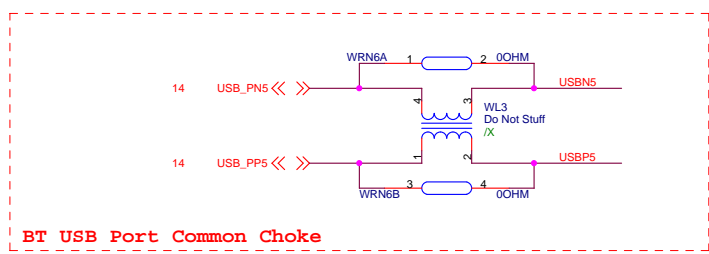
T91MT R1.0G 3.5G Module & External Antenna

ASUS		Title :	
ASUSTek Computer INC.		Engineer :	
Size A3	Project Name T91MT	Date Tuesday, July 07, 2009	Rev
		Sheet 23	of 57

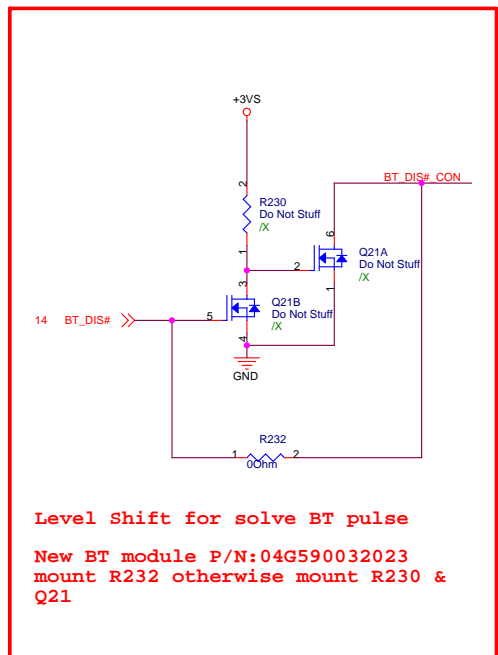


T91MT R1.0G

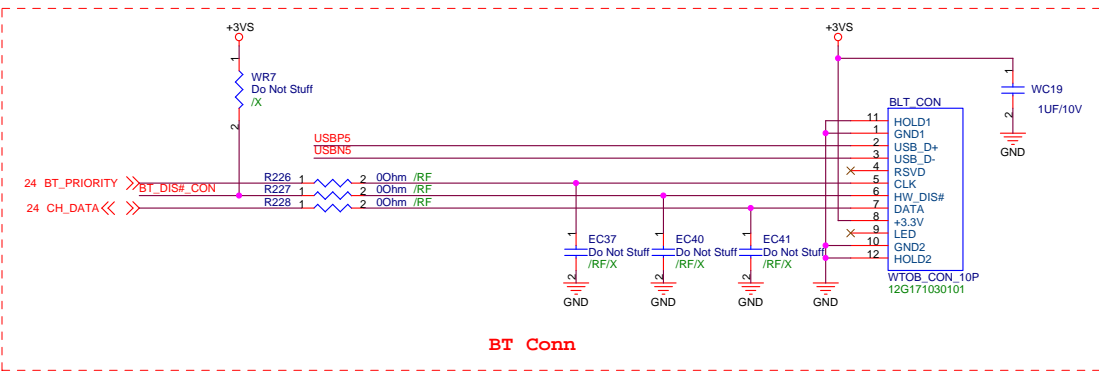
ASUS		Title : Mini WIFI	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
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Date: Tuesday, July 07, 2009	Sheet	24	of 57



BT USB Port Common Choke



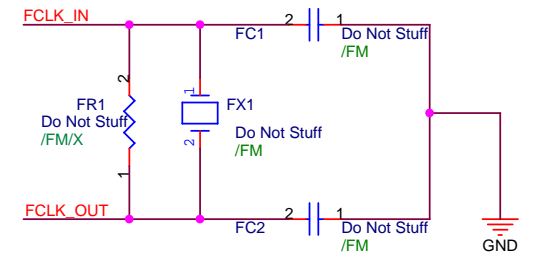
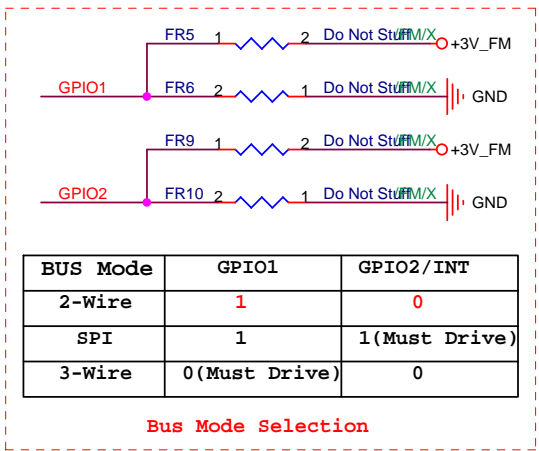
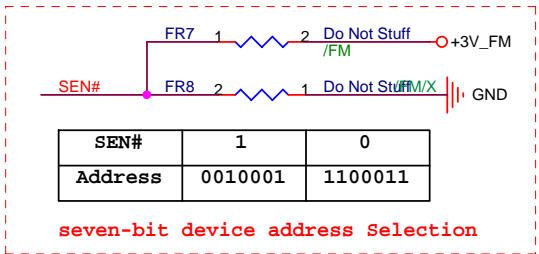
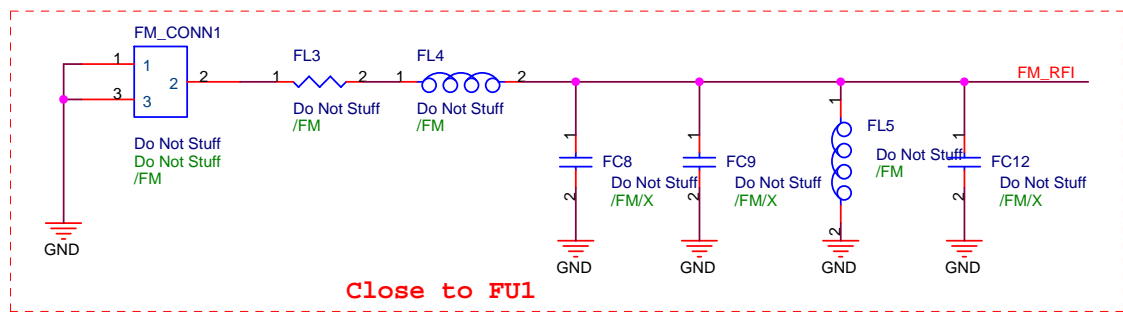
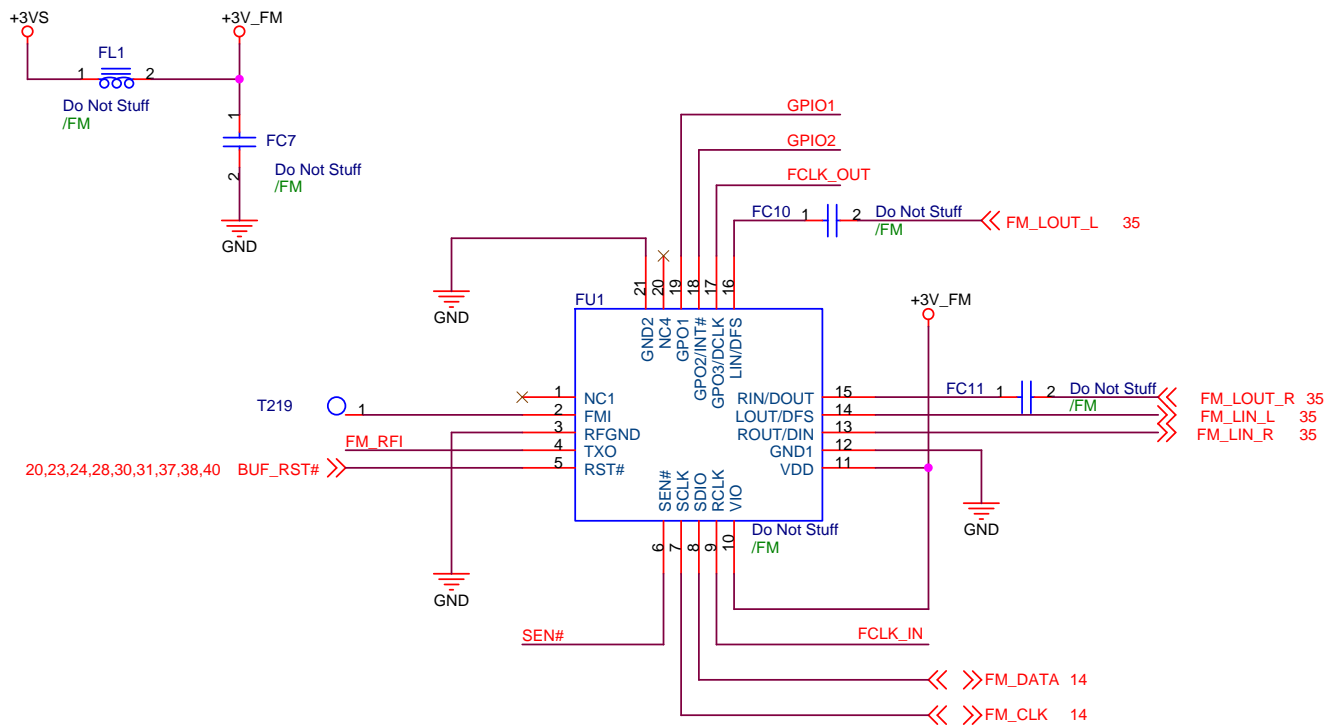
Level Shift for solve BT pulse
 New BT module P/N:04G590032023
 mount R232 otherwise mount R230 & Q21



BT Conn

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ASUS		Title : Bluetooth
ASUSTek Computer INC.		Engineer:
Size A3	Project Name T91MT	Rev
Date: Tuesday, July 07, 2009		Sheet 25 of 57



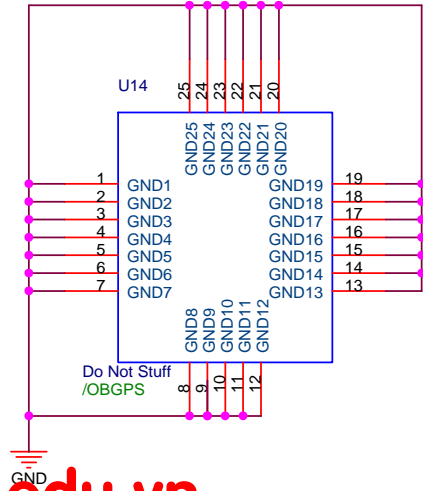
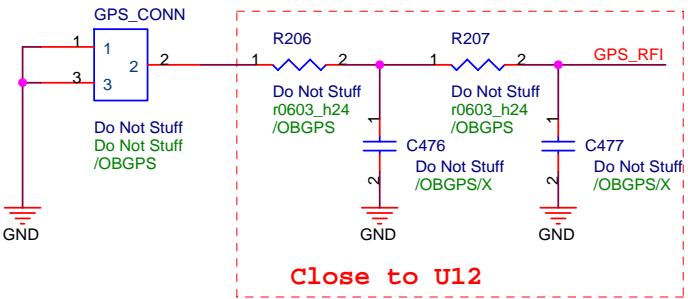
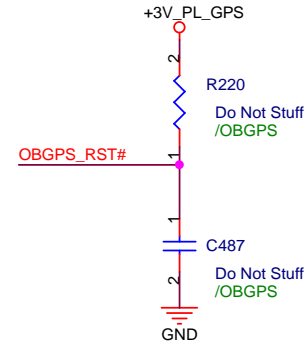
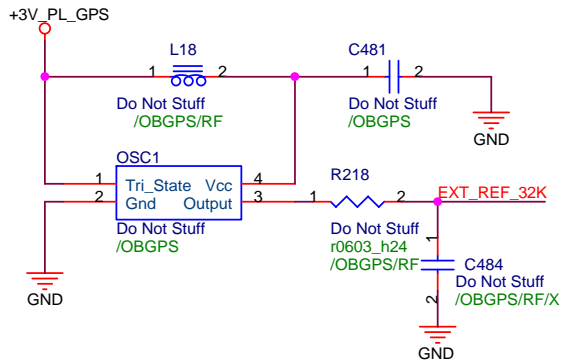
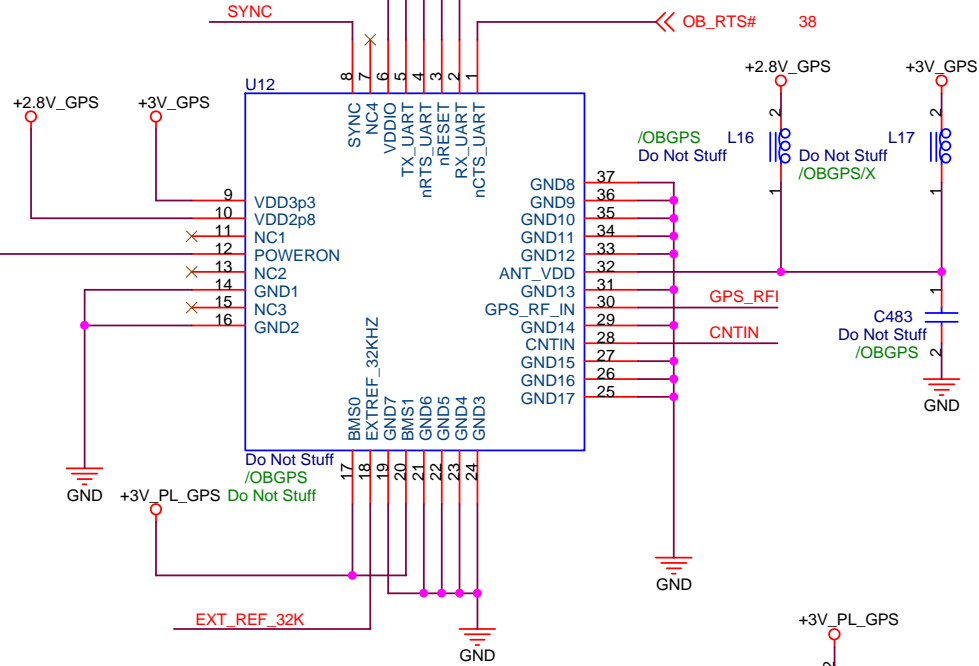
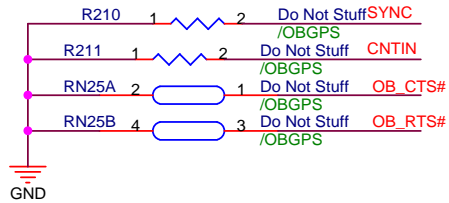
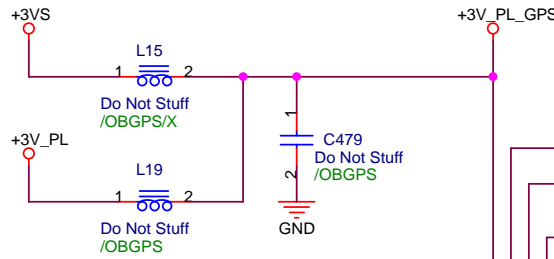
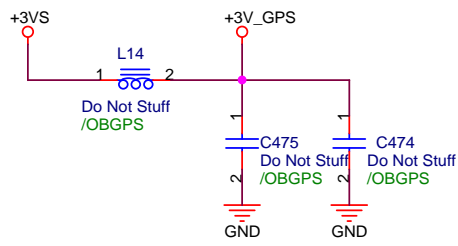
T91MT R1.0G

Title : FM RADIO

ASUSTek Computer INC. **Engineer:**

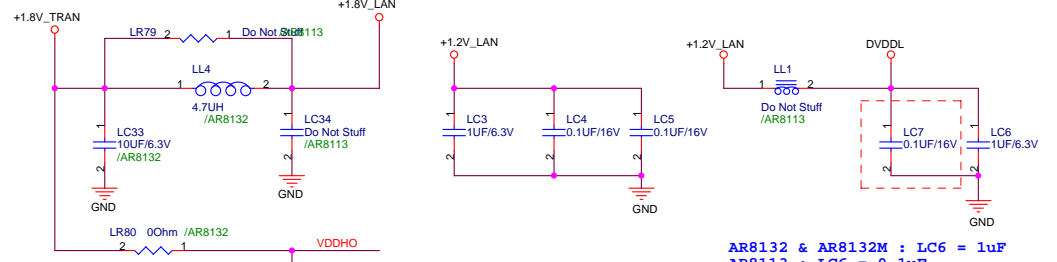
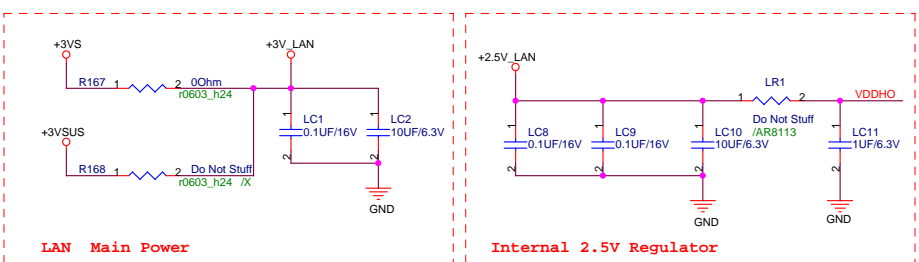
Size	Project Name	Rev
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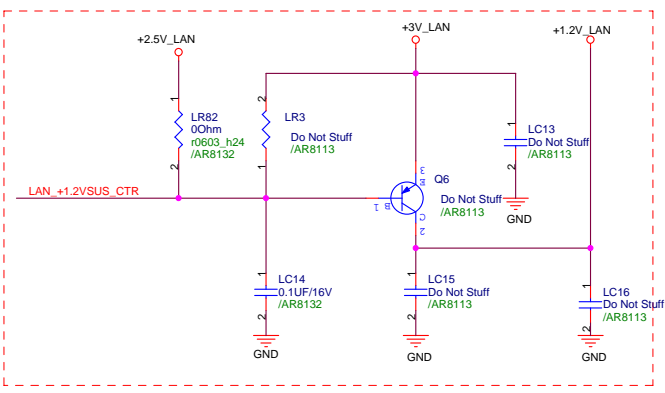


Close to U12

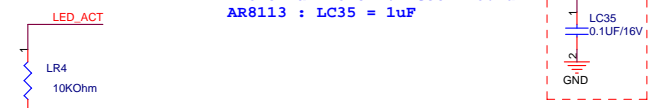
		Title : Onboard GPS	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
Custom	T91MT		
Date: Tuesday, July 07, 2009	Sheet 27	of 57	



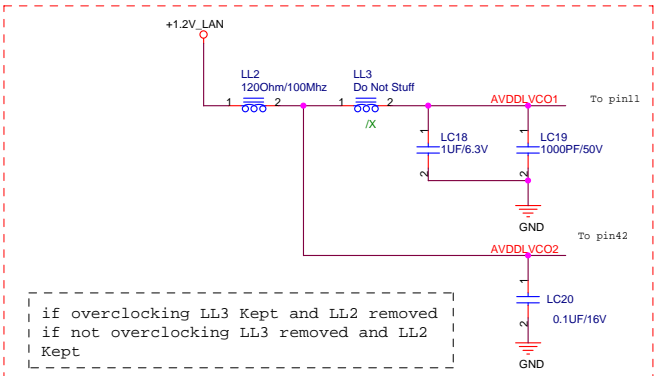
AR8132 & AR8132M : LC6 = 1uF
AR8113 : LC6 = 0.1uF



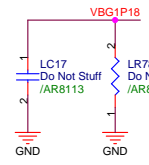
AR8132 & AR8132M: LC35 = 0.1uF
AR8113 : LC35 = 1uF



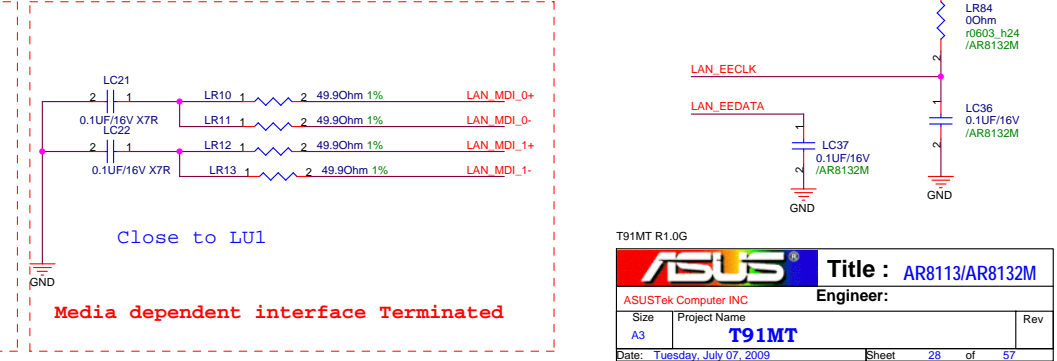
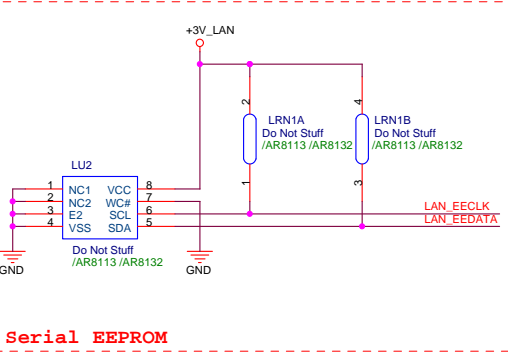
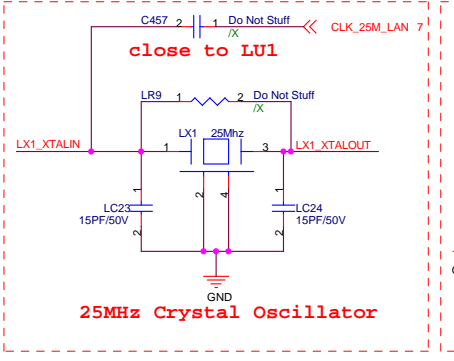
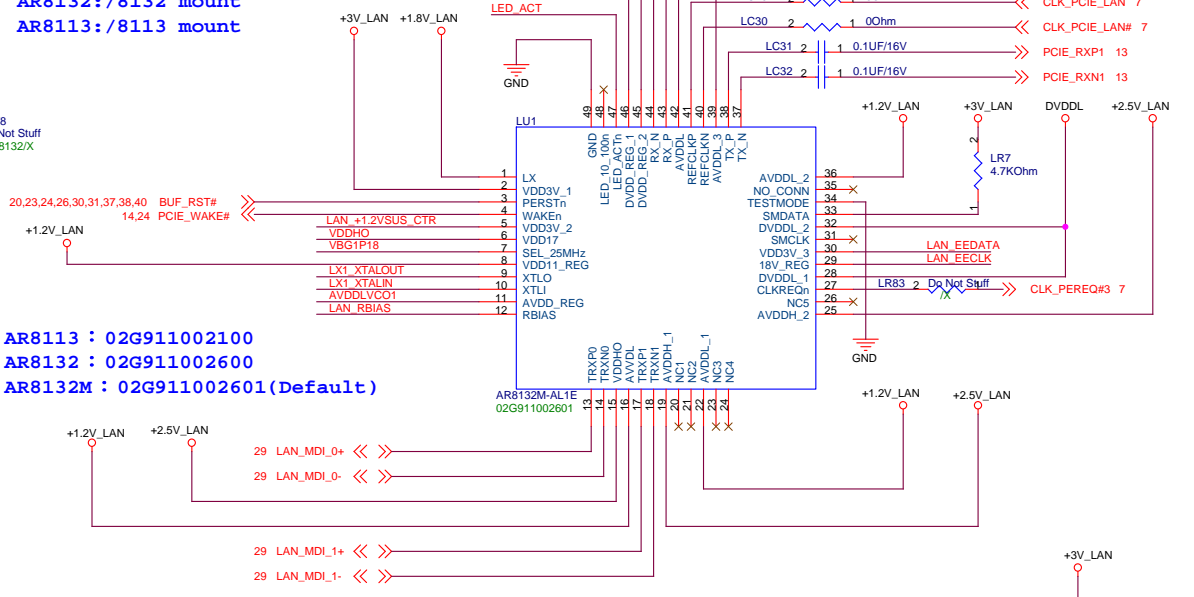
AR8132M:/8132+/8132M mount
AR8132:/8132 mount
AR8113:/8113 mount



if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept

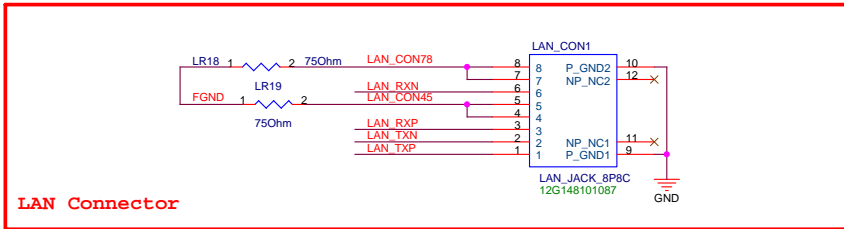
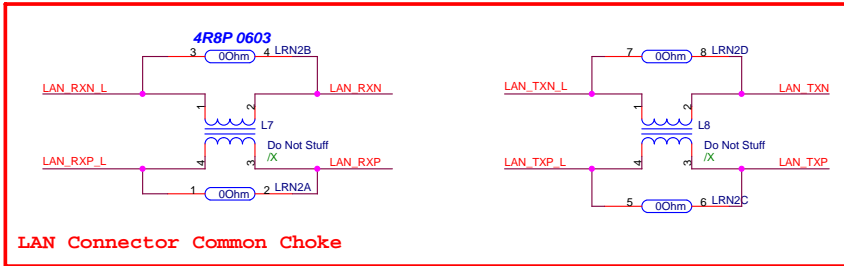
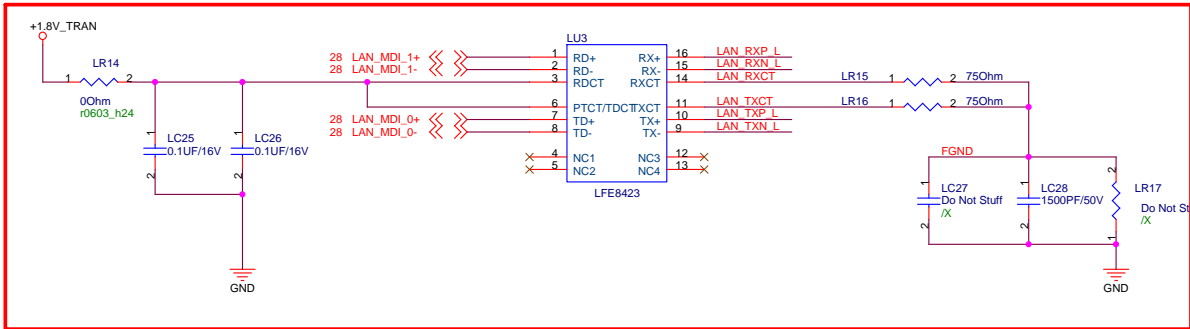


AR8113 : 02G911002100
AR8132 : 02G911002600
AR8132M : 02G911002601(Default)



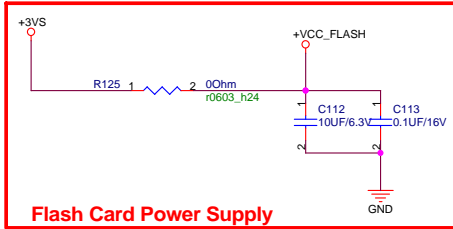
T91MT R1.0G

ASUS		Title : AR8113/AR8132M	
ASUSTek Computer INC		Engineer:	
Size	Project Name		Rev
A3	T91MT		
Date: Tuesday, July 07, 2009	Sheet 28 of 57		

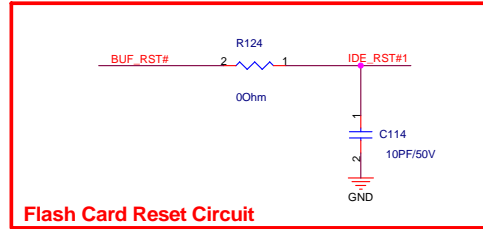


T91MT R1.0G

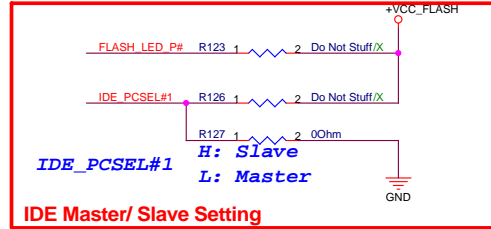
ASUS		Title : RJ45
ASUSTek Computer INC.		Engineer:
Size A3	Project Name T91MT	Rev
Date: Tuesday, July 07, 2009	Sheet 29	of 57



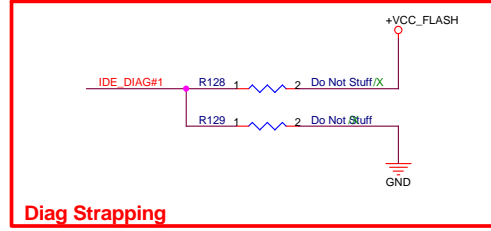
Flash Card Power Supply



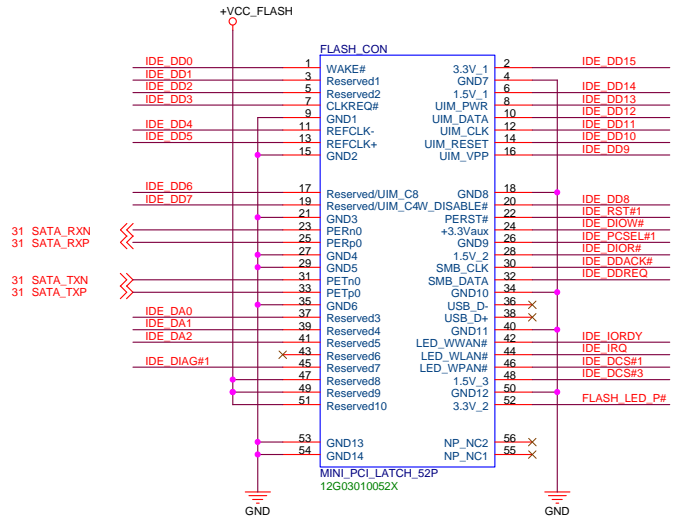
Flash Card Reset Circuit



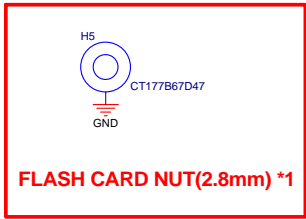
IDE Master/ Slave Setting



Diag Strapping



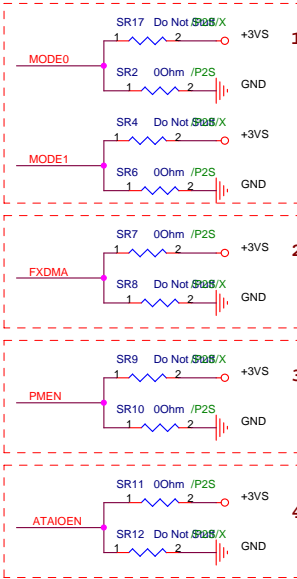
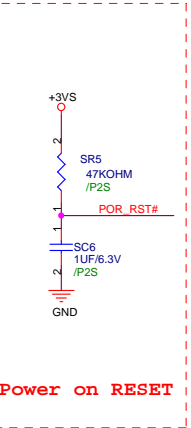
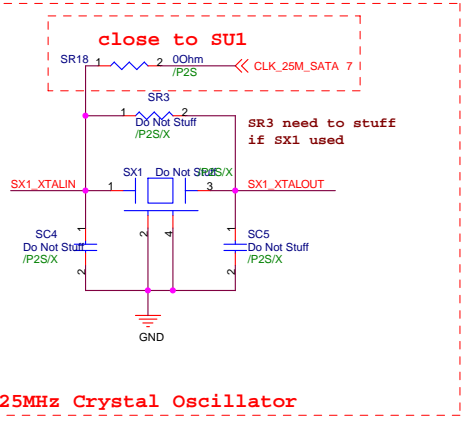
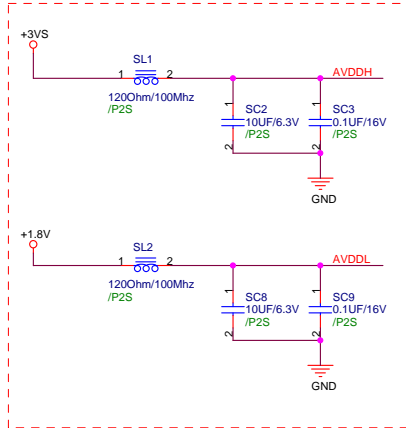
- << IDE_DD[15:0] 14,31
- >> IDE_DA[2:0] 14,31
- << IDE_DDACK# 14,31
- >> IDE_DDREQ 14,31
- << IDE_DIOR# 14,31
- >> IDE_DIOR# 14,31
- << IDE_DIOW# 14,31
- >> IDE_IORDY 14,31
- << IDE_DCS#1 14,31
- >> IDE_DCS#3 14,31
- << IDE_IRQ 14,31
- >> IDE_IRQ 14,31
- << BUF_RST# 20,23,24,26,28,31,37,38,40
- >> FLASH_LED_P# 31,43
- >> IDE_DIAG#1 31



FLASH CARD NUT(2.8mm) *1

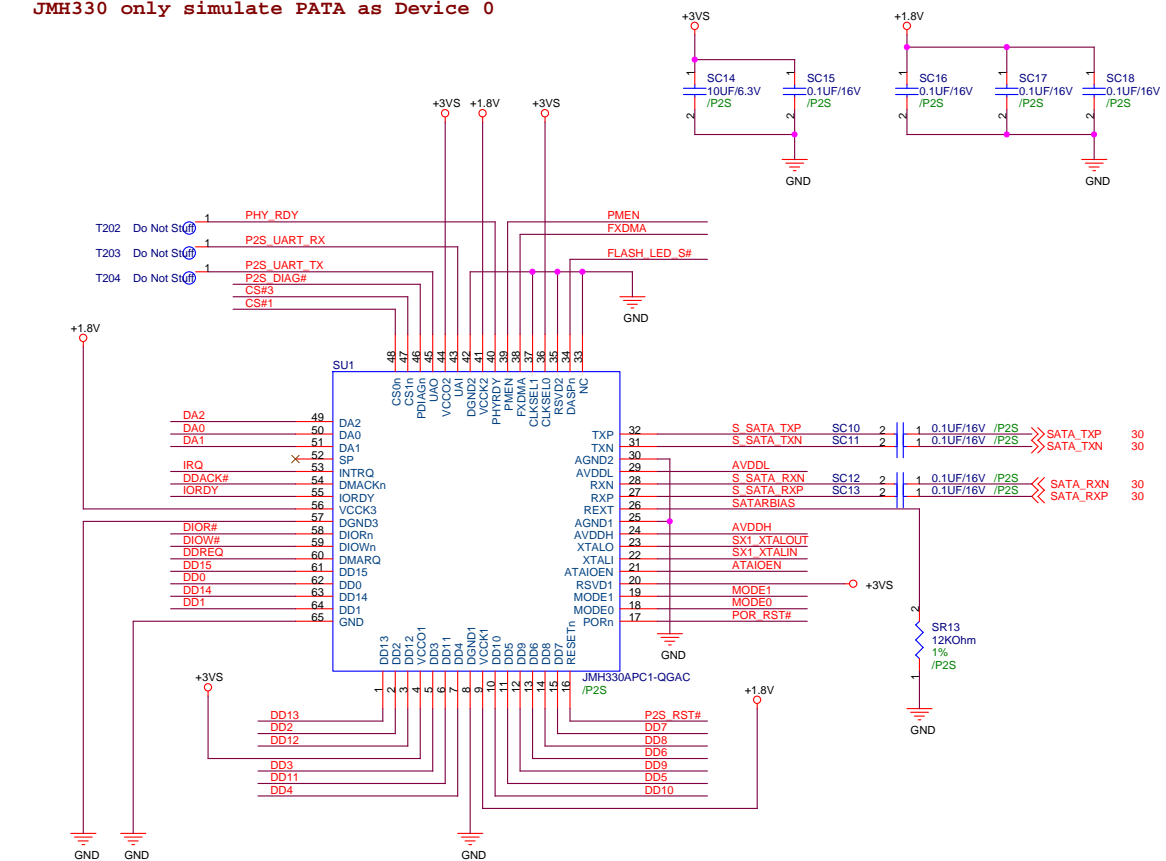
T91MT R1.0G

ASUS		Title : Flash Conn
ASUSTek Computer INC.		Engineer:
Size A3	Project Name T91MT	Rev
Date: Tuesday, July 07, 2009	Sheet 30 of 57	



- 1.MODE[1:0]=Select UDMA speed when FXDMA is set
00:100MB/s ; 01:133MB/s
10:150MB/s ; 11:Reserved
- 2.FXDMA=0,Auto adjustable speed rate according set Feature Command
FXDMA=1,speed rate depend on Mode[1:0] setting
- 3.PMEN=0 power management function Disable!
PMEN=1 power management function Enable!
- 4.ATAIOEN=0,Disable the ATA output pins, ATA I/O output pins are Hi-Z.
ATAIOEN=1,Enable ATA output

JMH330 only simulate PATA as Device 0



DD0	1	00HM	2	SRN1A /P2S	IDE DD0		
DD1	3	00HM	4	SRN1B /P2S	IDE DD1		
DD2	5	00HM	6	SRN1C /P2S	IDE DD2		
DD3	7	00HM	8	SRN1D /P2S	IDE DD3		
DD4	1	00HM	2	SRN2A /P2S	IDE DD4		
DD5	3	00HM	4	SRN2B /P2S	IDE DD5		
DD6	5	00HM	6	SRN2C /P2S	IDE DD6		
DD7	7	00HM	8	SRN2D /P2S	IDE DD7		
DD8	1	00HM	2	SRN3A /P2S	IDE DD8		
DD9	3	00HM	4	SRN3B /P2S	IDE DD9		
DD10	5	00HM	6	SRN3C /P2S	IDE DD10		
DD11	7	00HM	8	SRN3D /P2S	IDE DD11		
DD12	1	00HM	2	SRN4A /P2S	IDE DD12		
DD13	3	00HM	4	SRN4B /P2S	IDE DD13		
DD14	5	00HM	6	SRN4C /P2S	IDE DD14		
DD15	7	00HM	8	SRN4D /P2S	IDE DD15		
DD0	1	00HM	2	SRN5A /P2S	IDE DA0		
DA1	3	00HM	4	SRN5B /P2S	IDE DA1		
DA2	5	00HM	6	SRN5C /P2S	IDE DA2		
DA3	7	00HM	8	SRN5D /P2S	IDE DA3		
DDREQ	1	00HM	2	SRN6A /P2S	IDE DDREQ		>>> IDE_DDREQ 14,30
DIOW#	3	00HM	4	SRN6B /P2S	IDE DIOW#		>>> IDE_DIOW# 14,30
DIOR#	5	00HM	6	SRN6C /P2S	IDE DIOR#		>>> IDE_DIOR# 14,30
IORDY	7	00HM	8	SRN6D /P2S	IDE IORDY		>>> IDE_IORDY 14,30
CS#3	1	00HM	2	SRN7A /P2S	IDE DCS#3		>>> IDE_DCS#3 14,30
CS#1	3	00HM	4	SRN7B /P2S	IDE DCS#1		>>> IDE_DCS#1 14,30
DDACK#	5	00HM	6	SRN7C /P2S	IDE DDACK#		>>> IDE_DDACK# 14,30
IRQ	7	00HM	8	SRN7D /P2S	IDE IRQ		>>> IDE_IRQ 14,30
P2S_DIAG#	1	00hm	2	IDE DIAG#1			<<< IDE_DIAG#1 30
P2S_RST#	1	00hm	2	BUF_RST#			<<< BUF_RST# 20,23,24,26,28,30,37,38,40
FLASH_LED_S#	1	00hm	2	FLASH_LED_P#			<<< FLASH_LED_P# 30,43 >>> FLASH_LED_S# 43

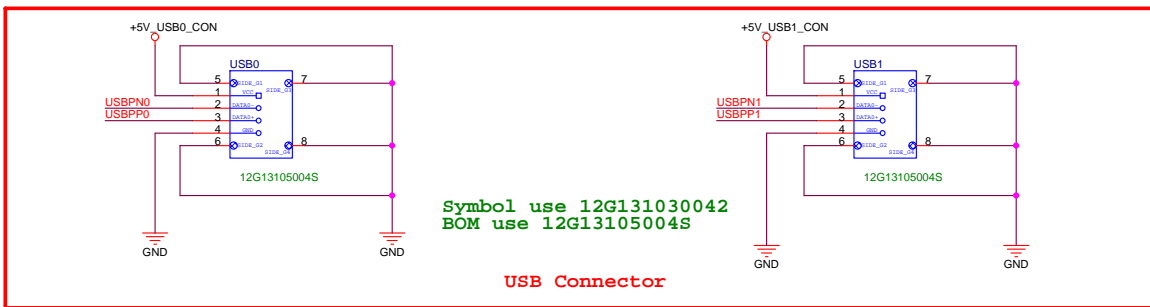
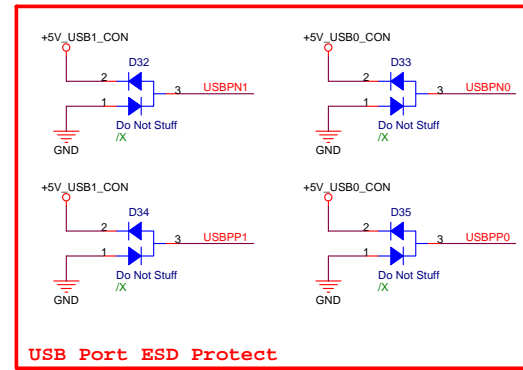
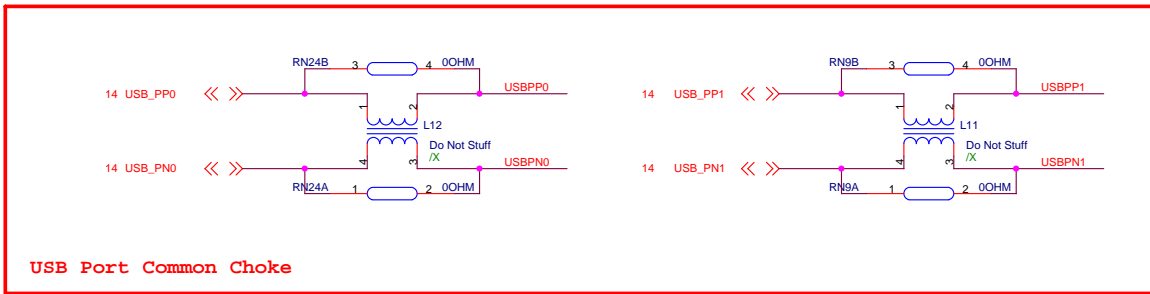
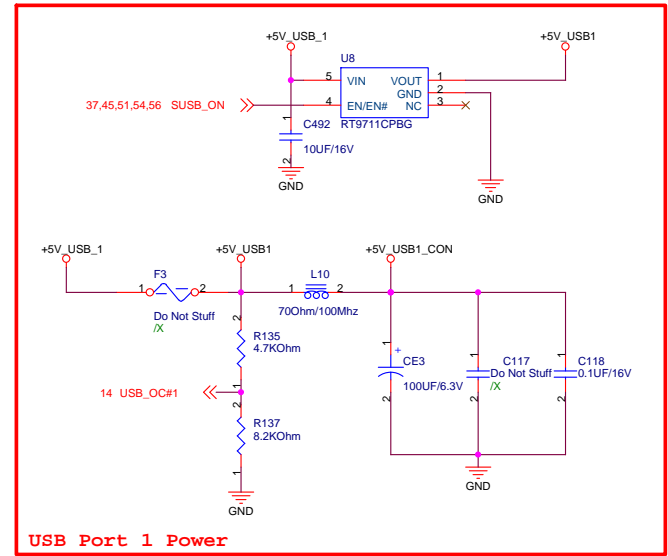
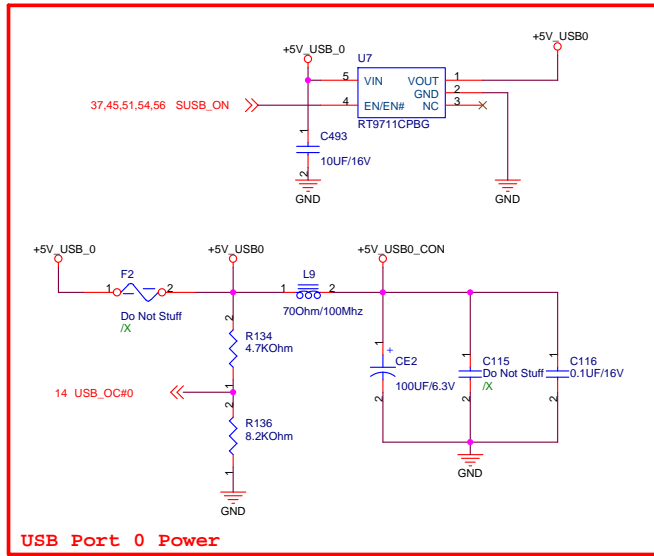
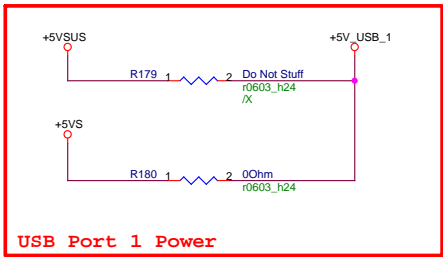
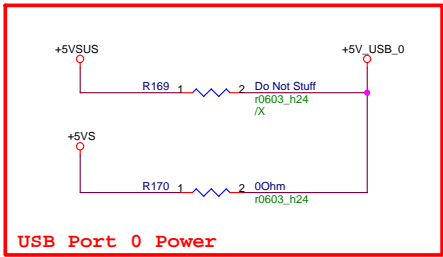
T91MT R1.0G

Title : PATA to SATA

ASUSTek Computer INC. **Engineer:**

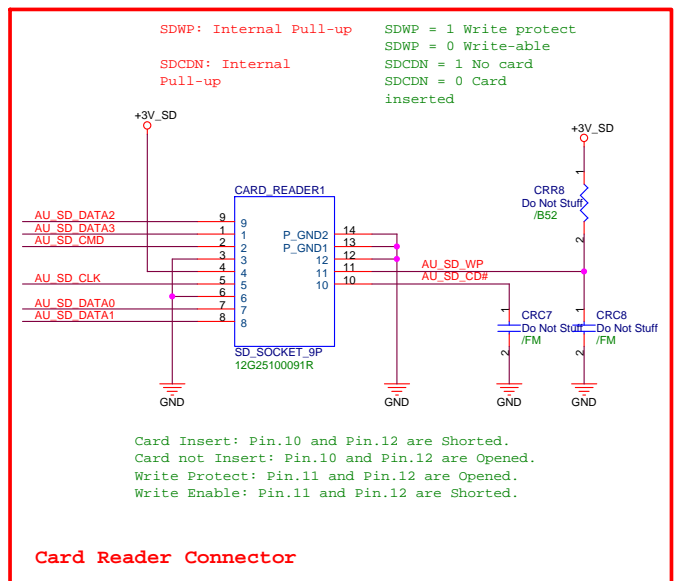
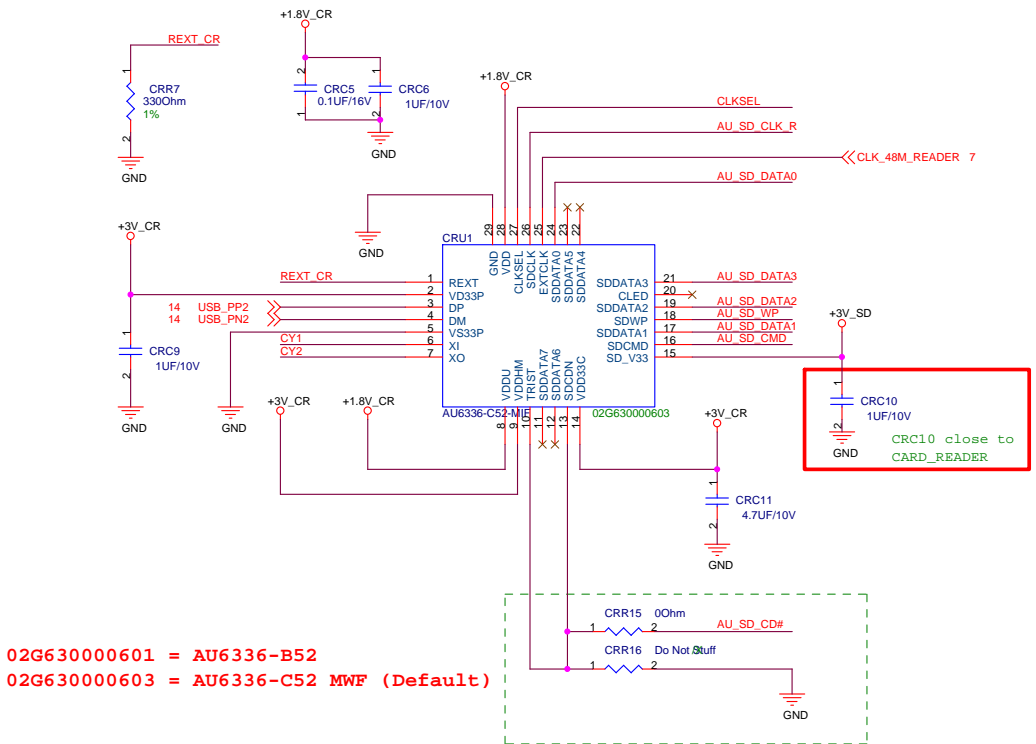
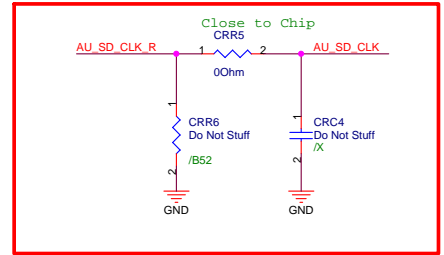
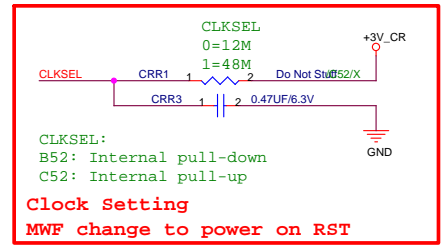
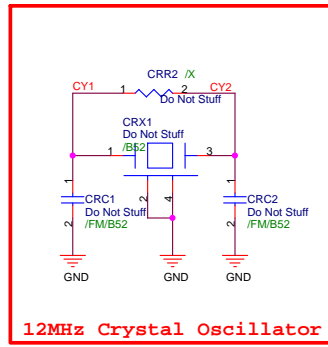
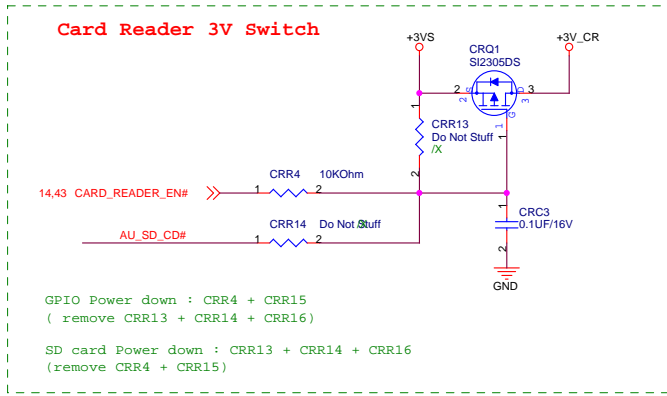
Size	Project Name	Rev
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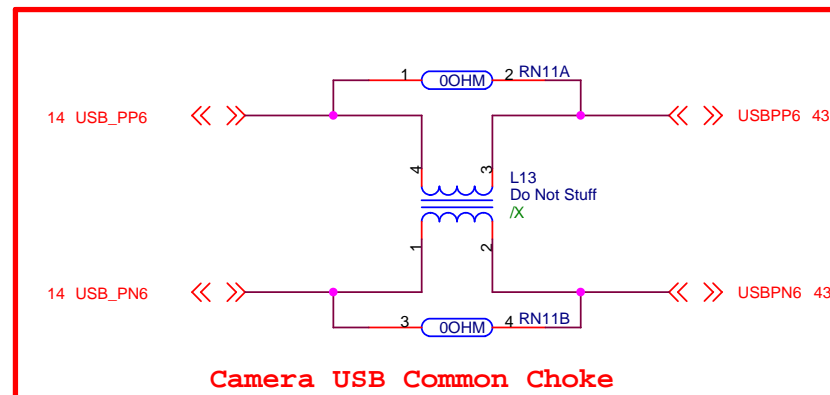
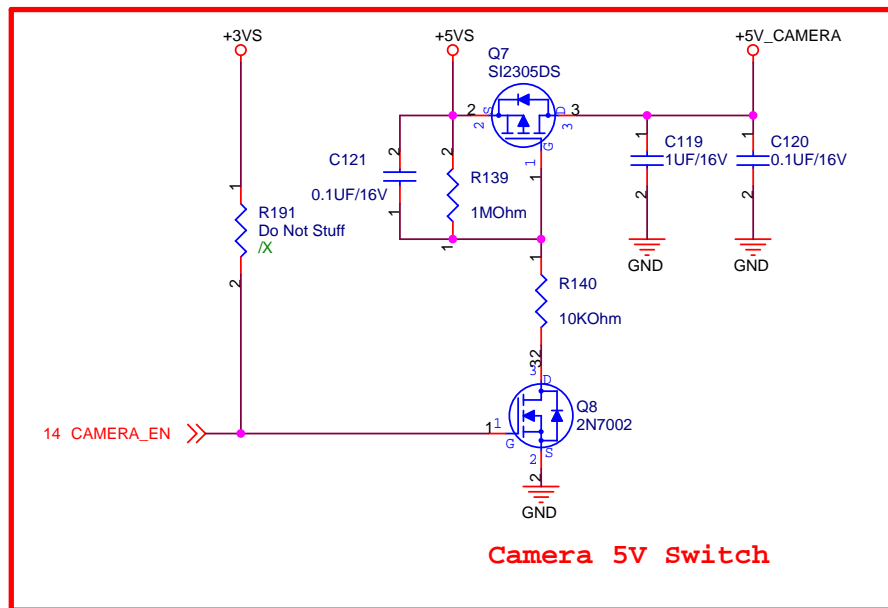
T91MT R1.0G

ASUS		Title : USB Port	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
A3	T91MT		
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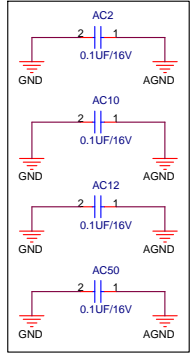
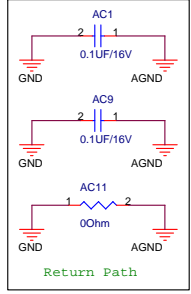
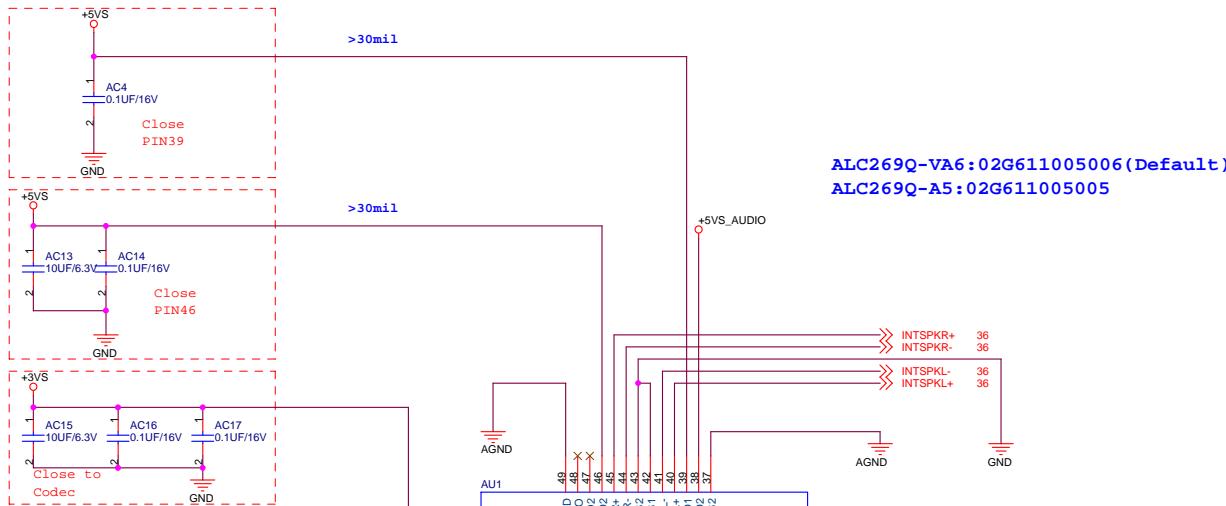
T91MT R1.0G

ASUS		Title : AU6336-C52	
ASUSTek Computer Inc.		Engineer:	
Size	Project Name	T91MT	
Date	Tuesday, July 07, 2009	Sheet	33 of 57

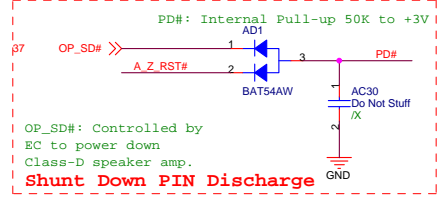
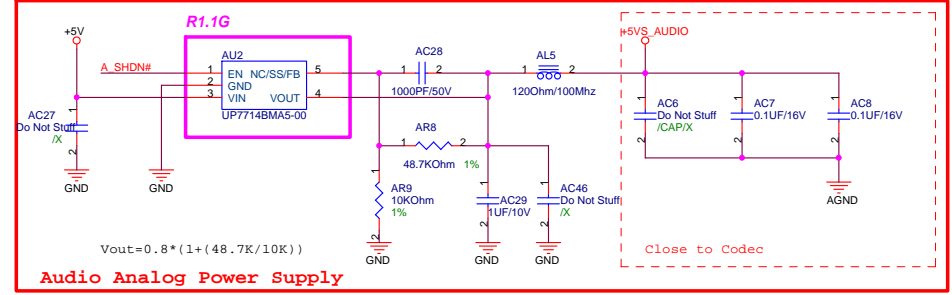
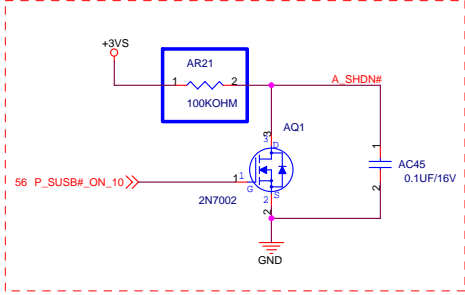
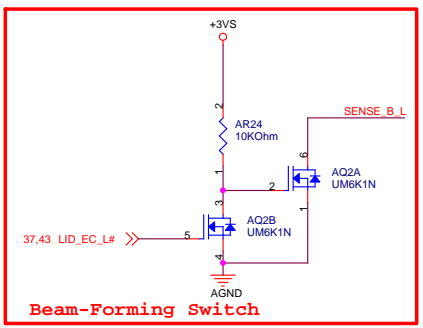
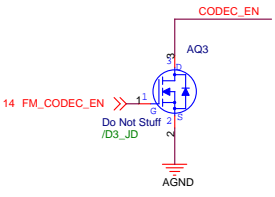


T91MT R1.0G

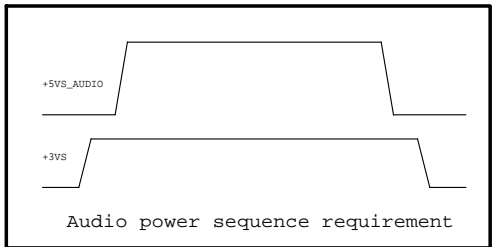
		Title : Camera Conn	
ASUSTek Computer INC.		Engineer:	
Size A4	Project Name T91MT		Rev
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/D3_JD : Disable D3 by Jack detecting
/D3_AP : Disable D3 by AP and Driver

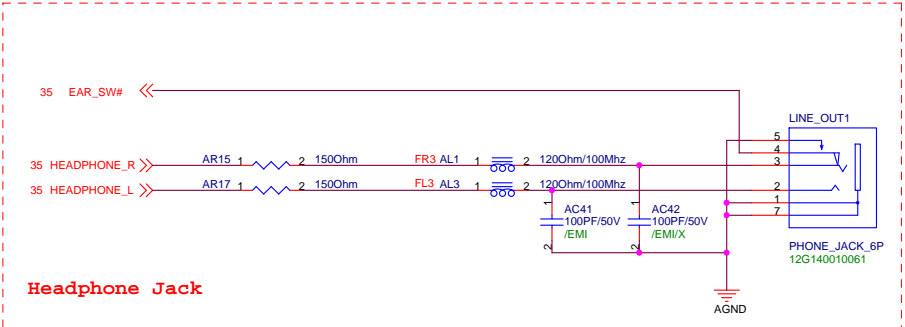
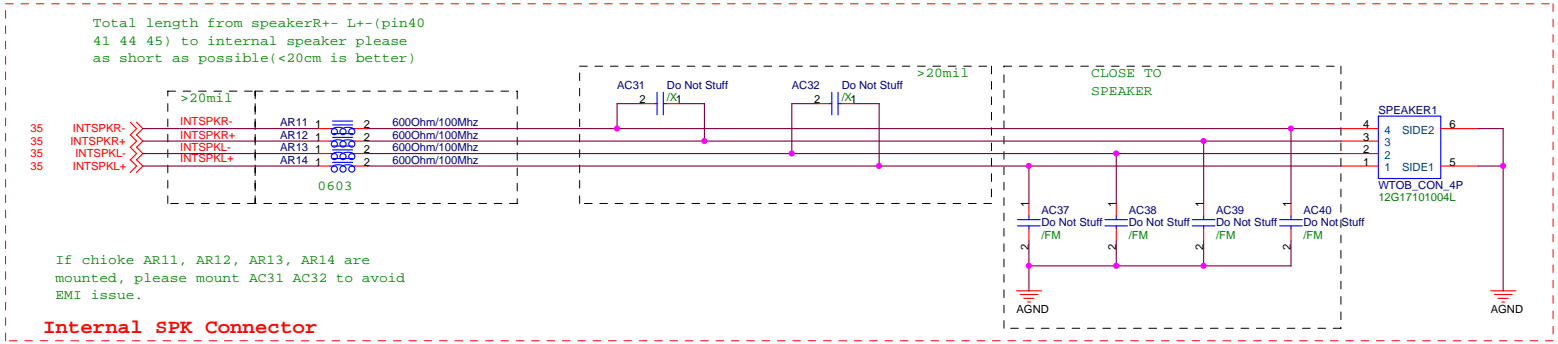


Need 4.7u/10v X5R to prevent poor THD+N
Analog: Pin.13-Pin.38
Digital: Pin.1-Pin.12 and Pin.39-Pin.48

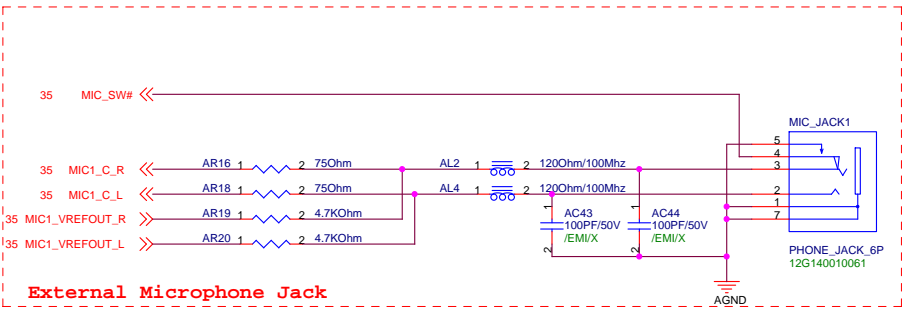


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ASUS		Title : ALC269-1	
ASUSTek Computer Inc.		Engineer:	
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Custom		Date: Tuesday, July 07, 2009	Sheet 35 of 57

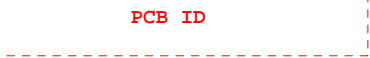
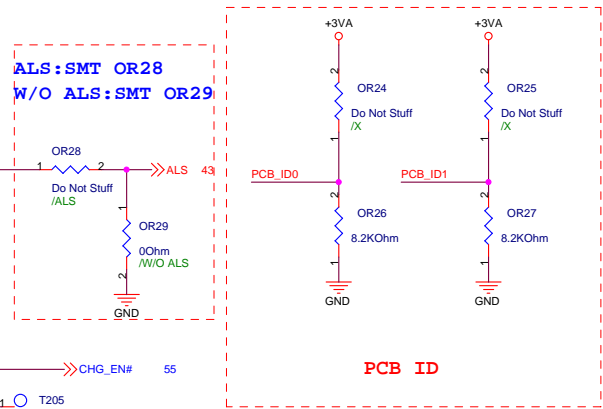
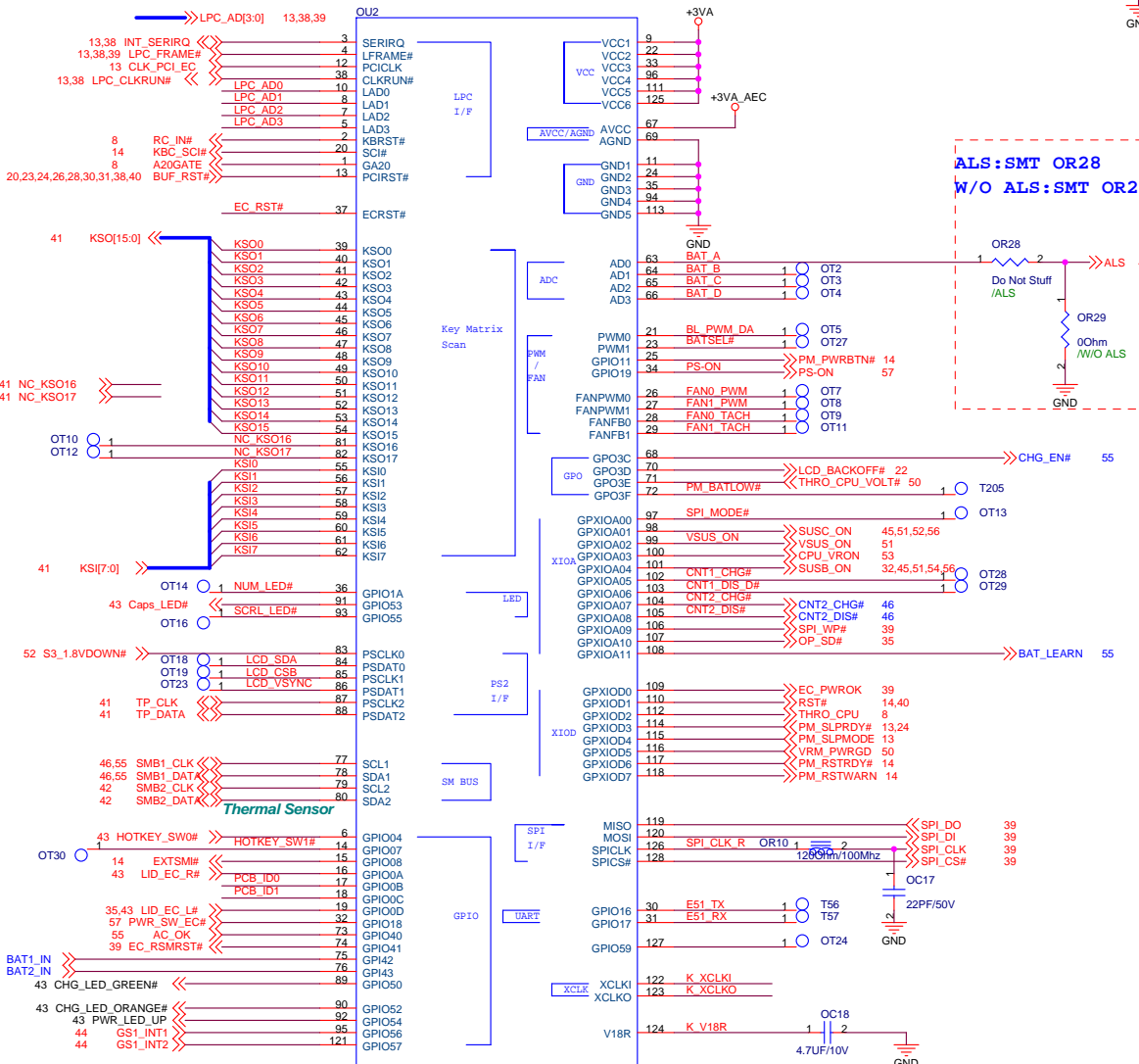
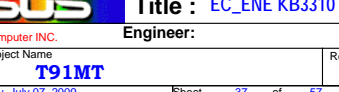
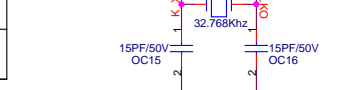
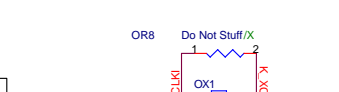
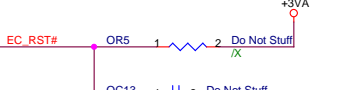
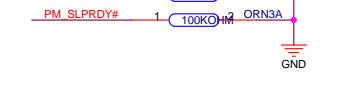
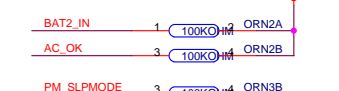
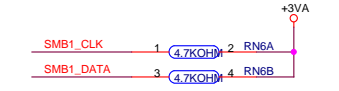
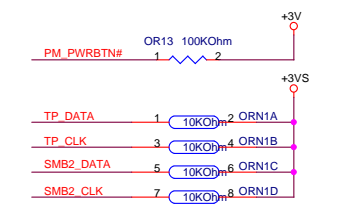
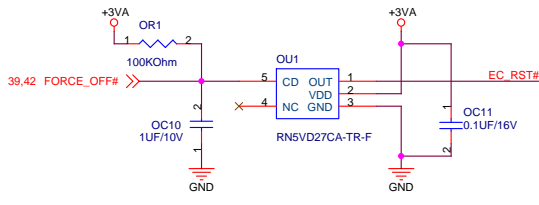
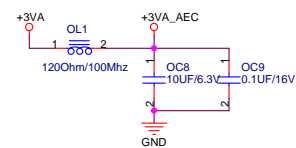
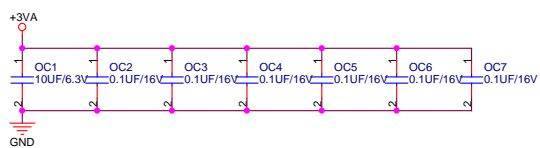


Symbol use 12G140010060
BOM use 12G140010061



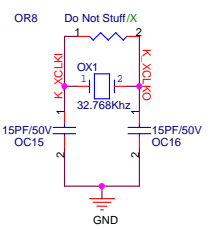
T91MT R1.0G

ASUS		Title : ALC269-2	
ASUSTek Computer Inc.		Engineer:	
Size A3	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009	Sheet 36	of 57	



Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home



C1版 : 02G890000712 OC18: 4.7U (Default)
 A0版 : 02G890000700 OC18: 1U

HOTKEY_SW0# - HOTKEY_SW3# internal PU

T91MT R1.0G

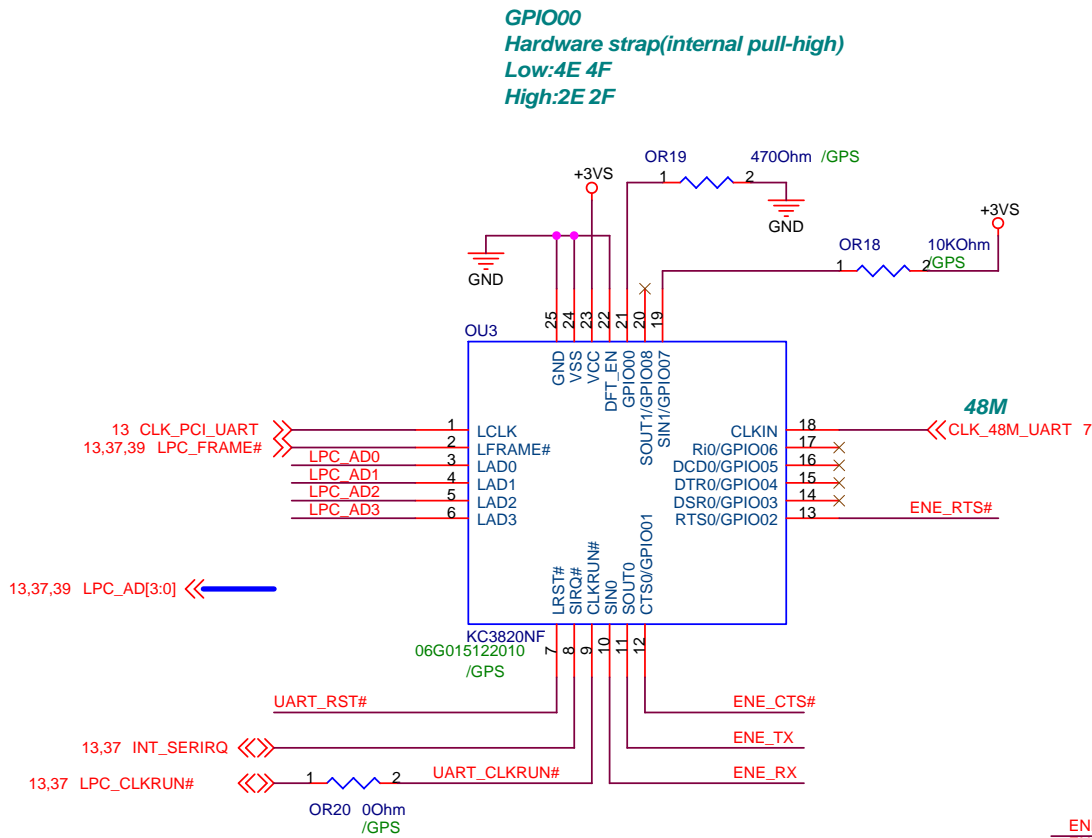
ASUS Title : EC_ENE KB3310

ASUSTek Computer INC. Engineer:

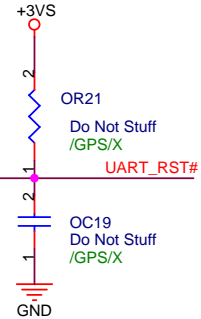
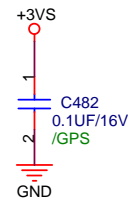
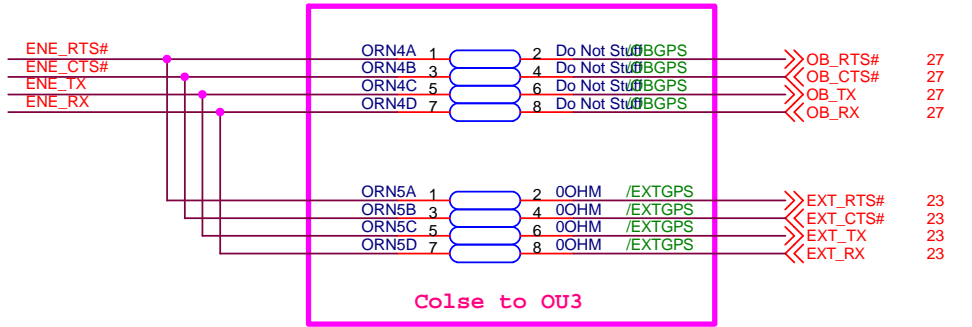
Size	Project Name	Rev
A3	T91MT	

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GPIO00
 Hardware strap(internal pull-high)
 Low:4E 4F
 High:2E 2F



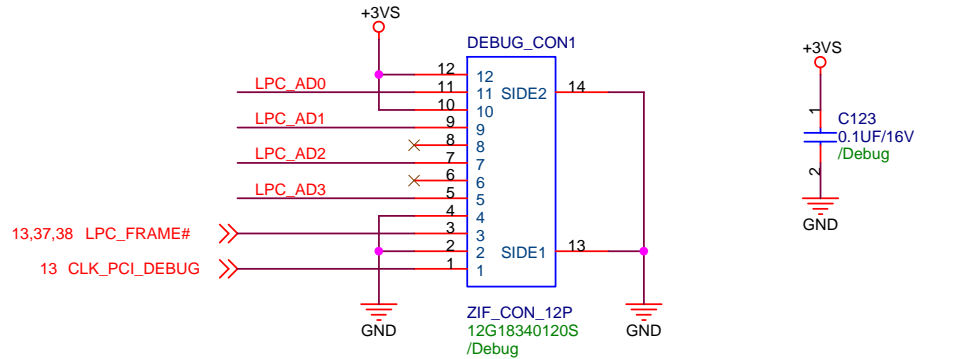
UART Control IC for using GPS module
 due to no UART on ENE EC



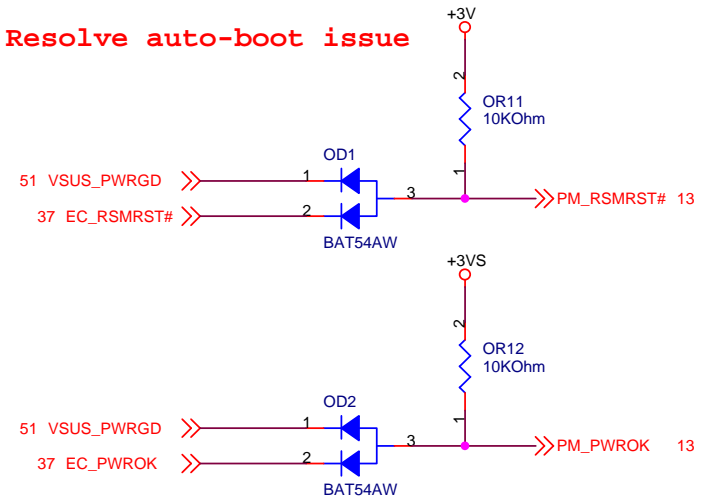
T91MT R1.0G

ASUS		Title : EC_UART_KC3820	
ASUSTek Computer INC.		Engineer:	
Size A4	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009		Sheet 38 of 57	

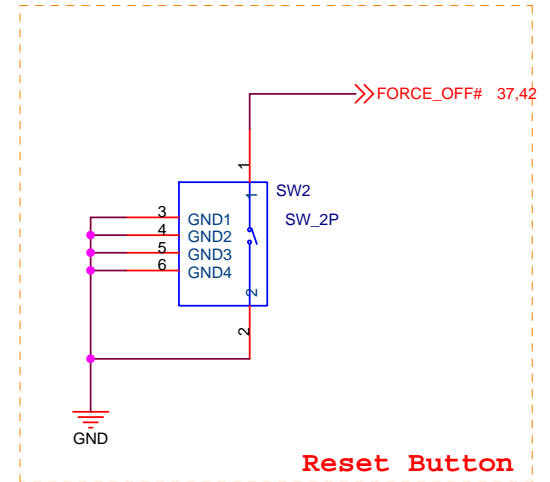
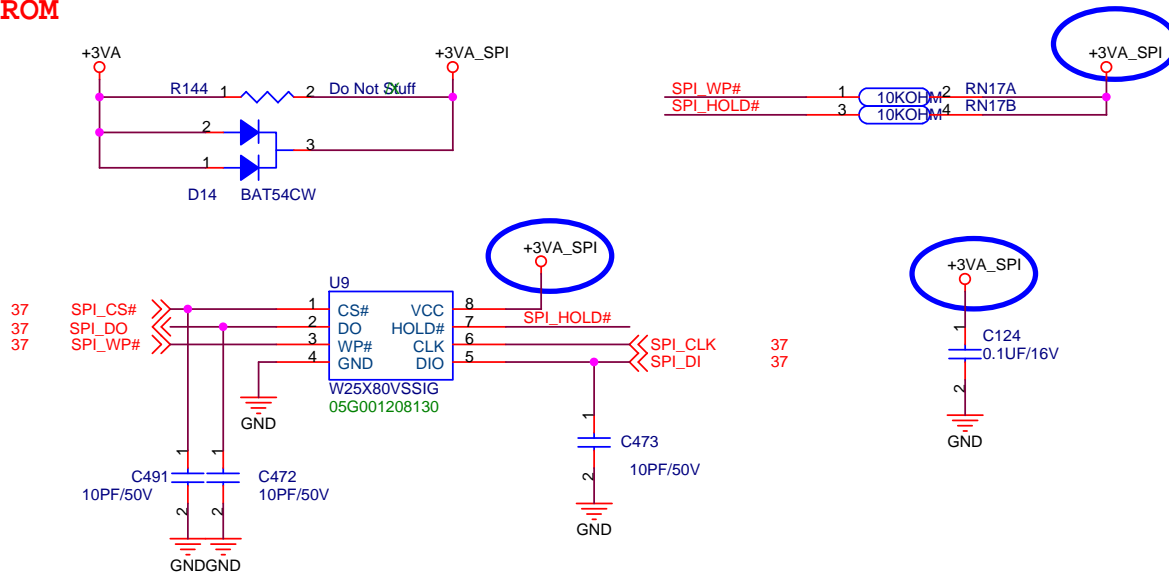
For Debug



Resolve auto-boot issue

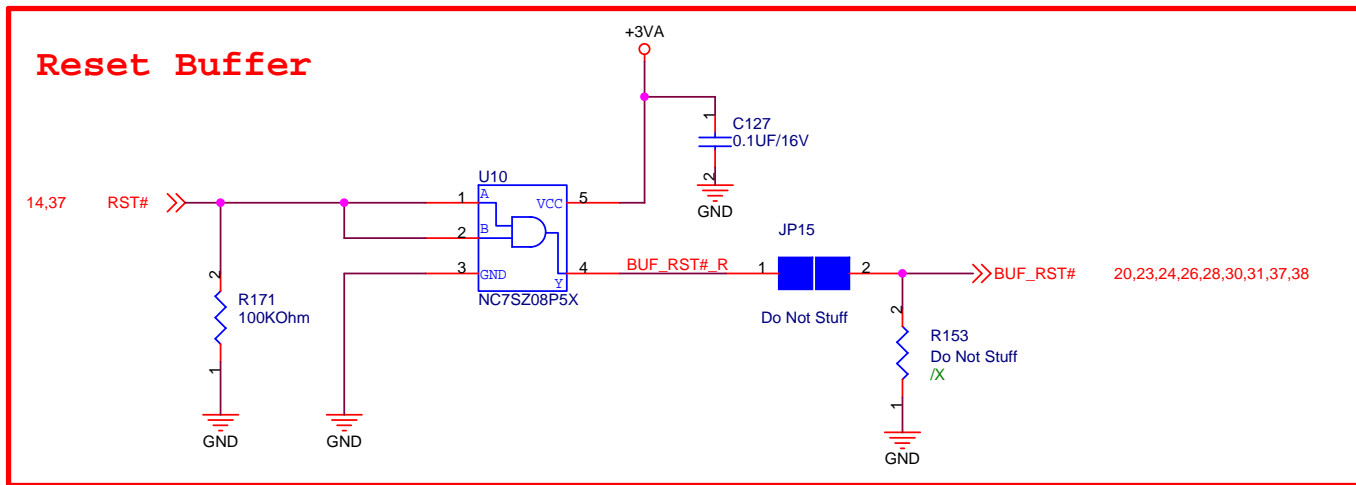
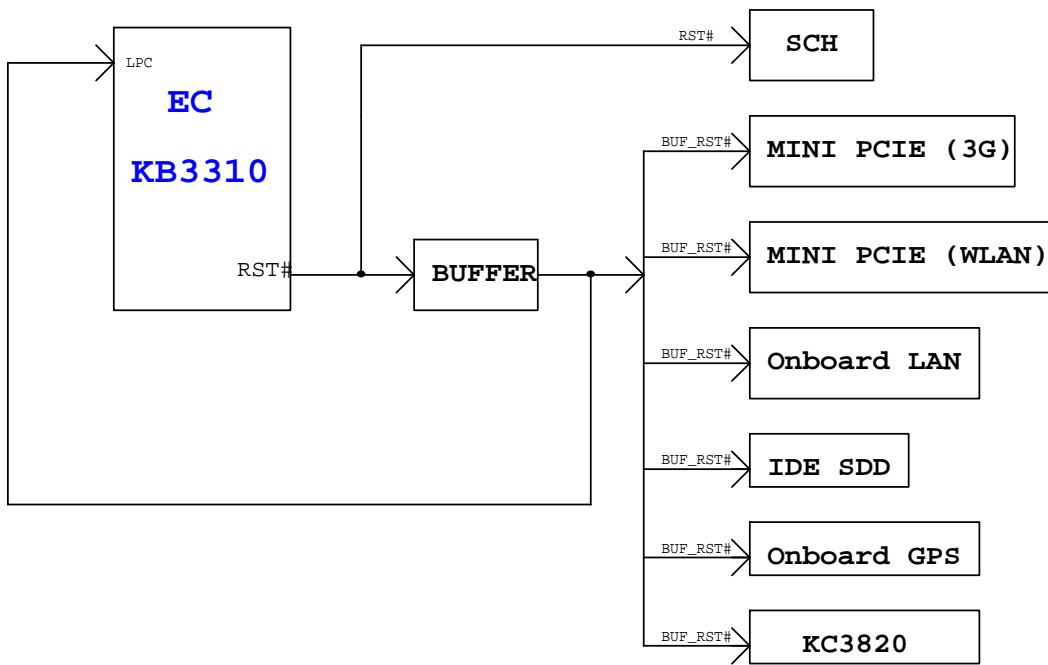


SPI ROM



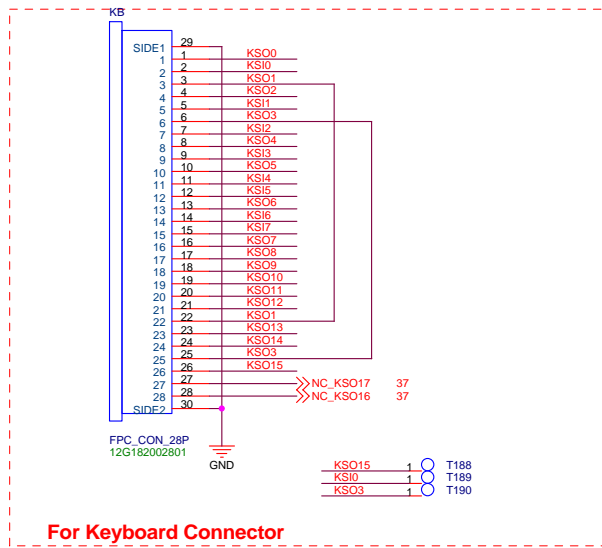
T91MT R1.0G

		Title : SPI ROM/ Debug
ASUSTek Computer INC.		Engineer:
Size A4	Project Name T91MT	Rev
Date: Tuesday, July 07, 2009		Sheet 39 of 57

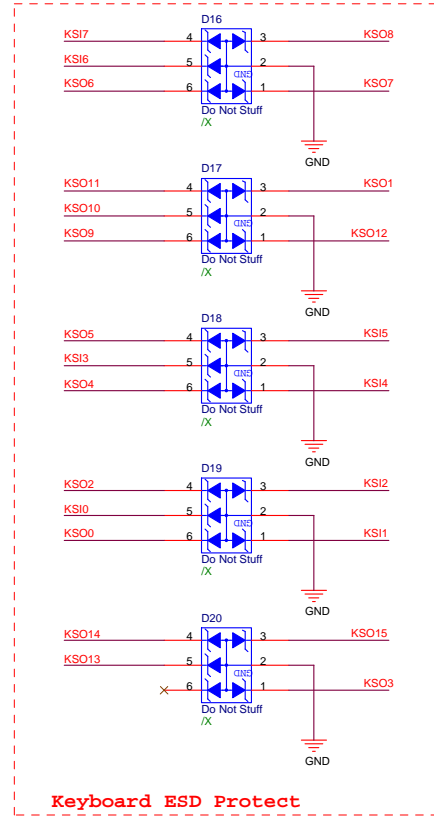
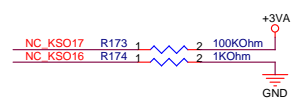


T91MT R1.0G

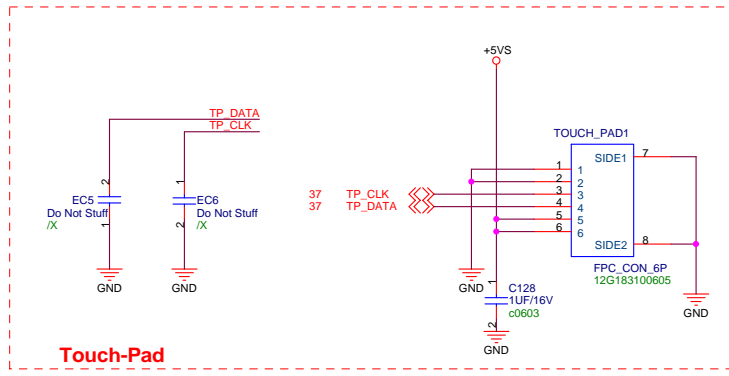
ASUS		Title : Reset Map	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009		Sheet	40 of 57



For Keyboard Connector



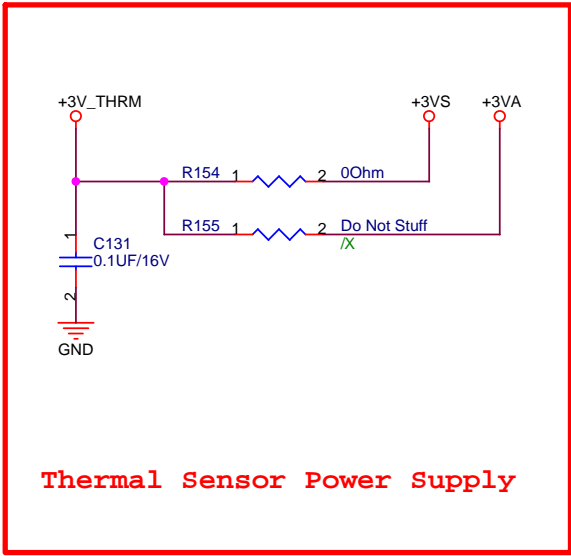
Keyboard ESD Protect



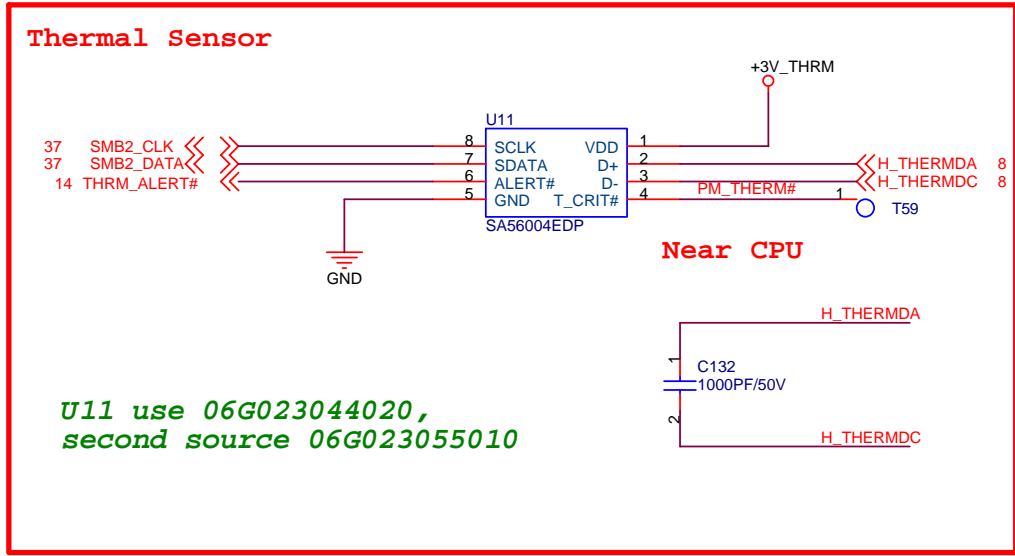
Touch-Pad

T91MT R1.0G

ASUS		Title : KB_Touch Pad
ASUSTek Computer INC.		Engineer:
Size A3	Project Name T91MT	Rev
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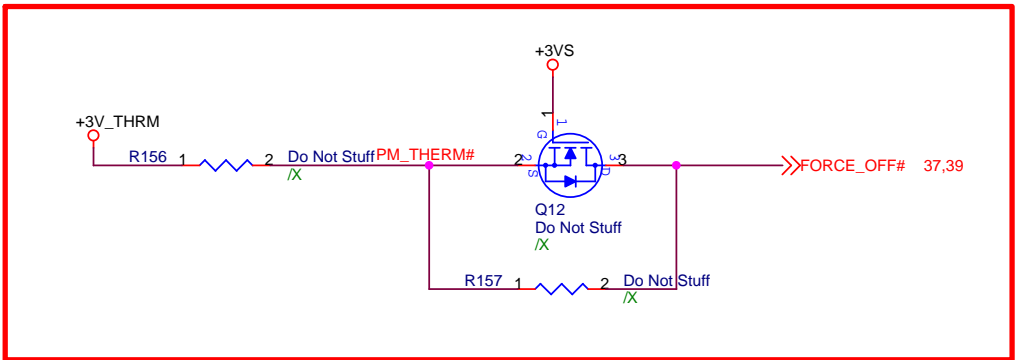
Thermal Sensor Power Supply



Thermal Sensor

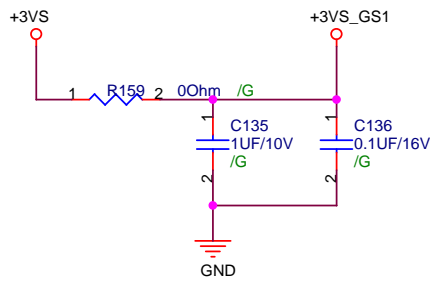
U11 use 06G023044020,
second source 06G023055010

Near CPU

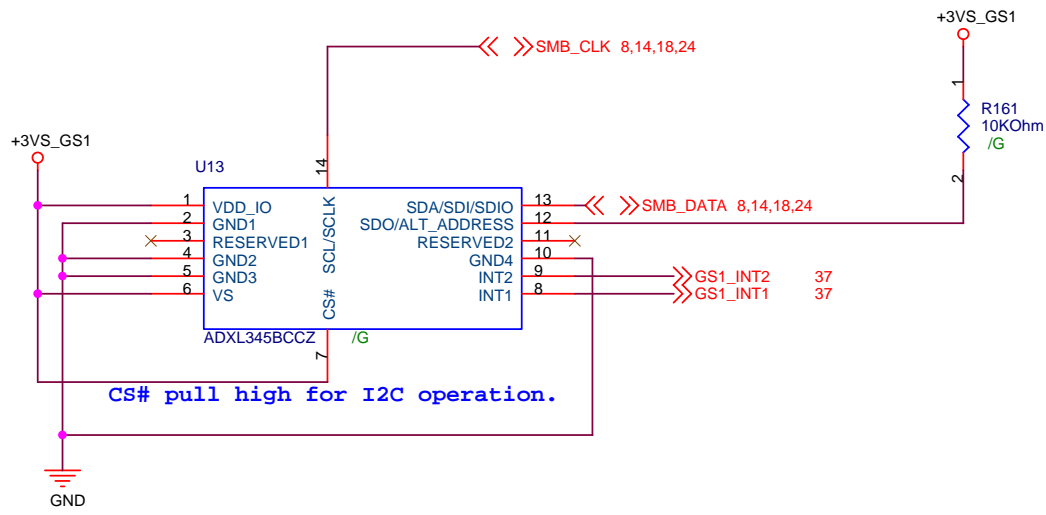


T91MT R1.0G

		Title : Thermal Sensor	
ASUSTek Computer INC.		Engineer:	
Size A4	Project Name T91MT		Rev
Date: Tuesday, July 07, 2009		Sheet 42 of 57	

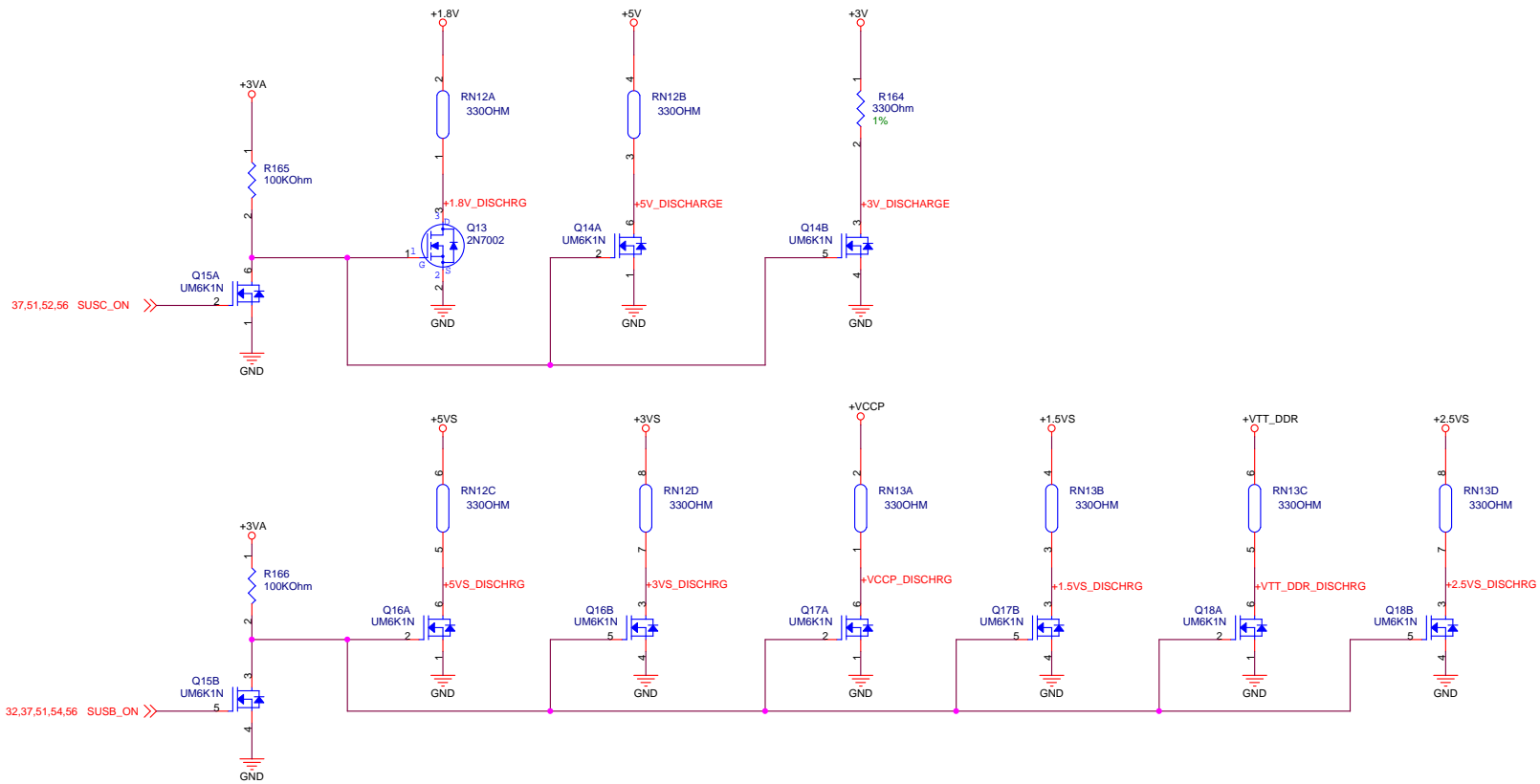


SMBUS Address: 0X1D



T91MT R1.0G

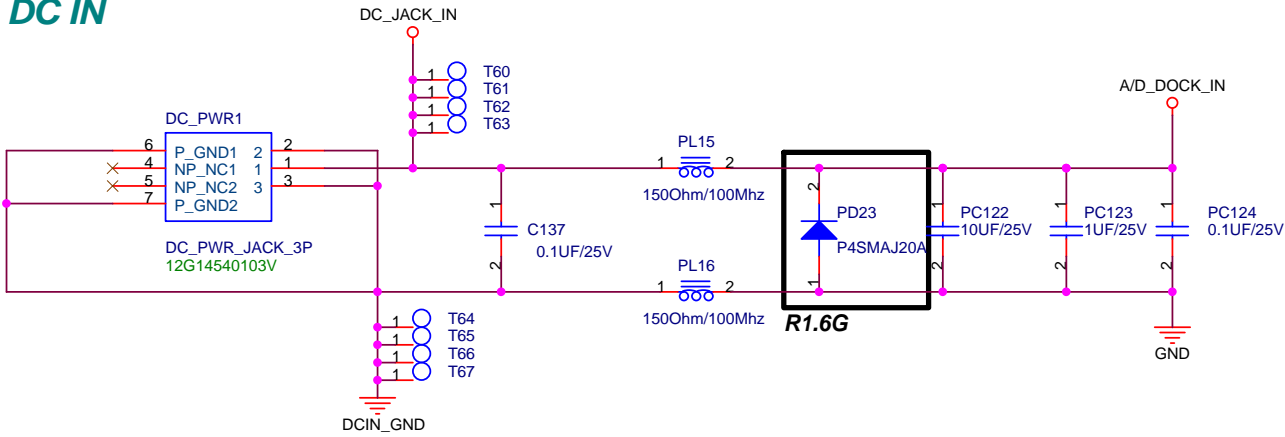
		Title : G-Sensor	
ASUSTek Computer INC.		Engineer:	
Size A4	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009		Sheet	44 of 57



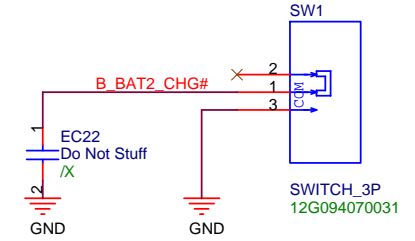
T91MT R1.0G

ASUS		Title : Discharge
ASUSTek Computer INC.		Engineer:
Size A3	Project Name T91MT	Rev
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DC IN

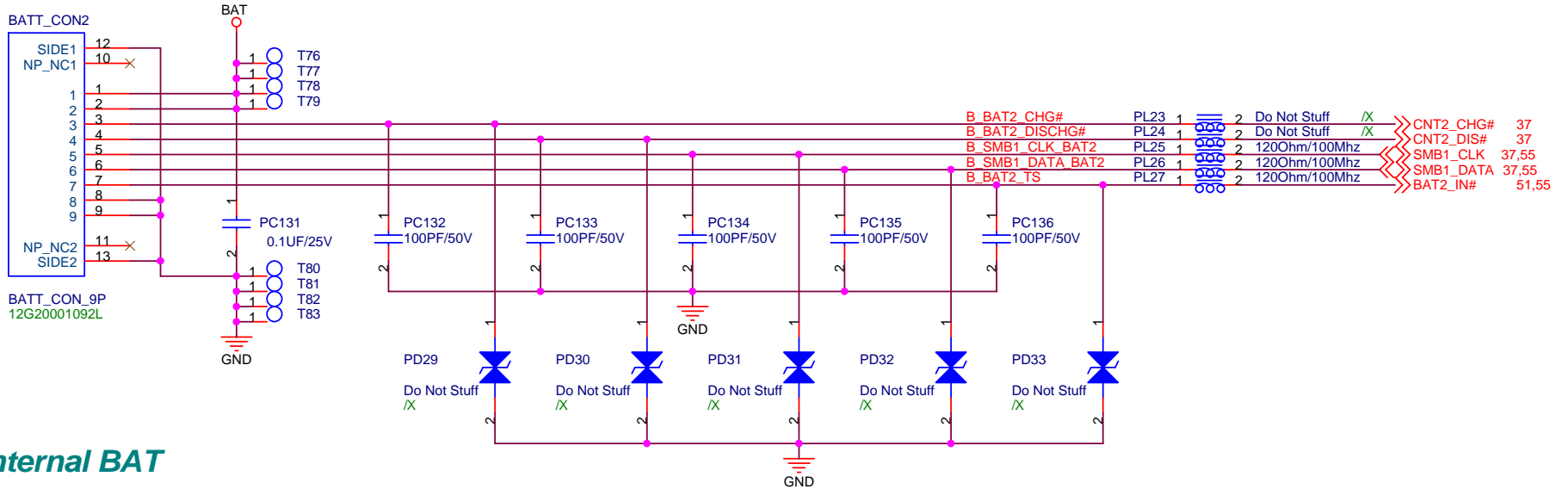


Battery Switch



CNT2_CHG# : Low : Battery ON
 CNT2_CHG# : open : Battery OFF

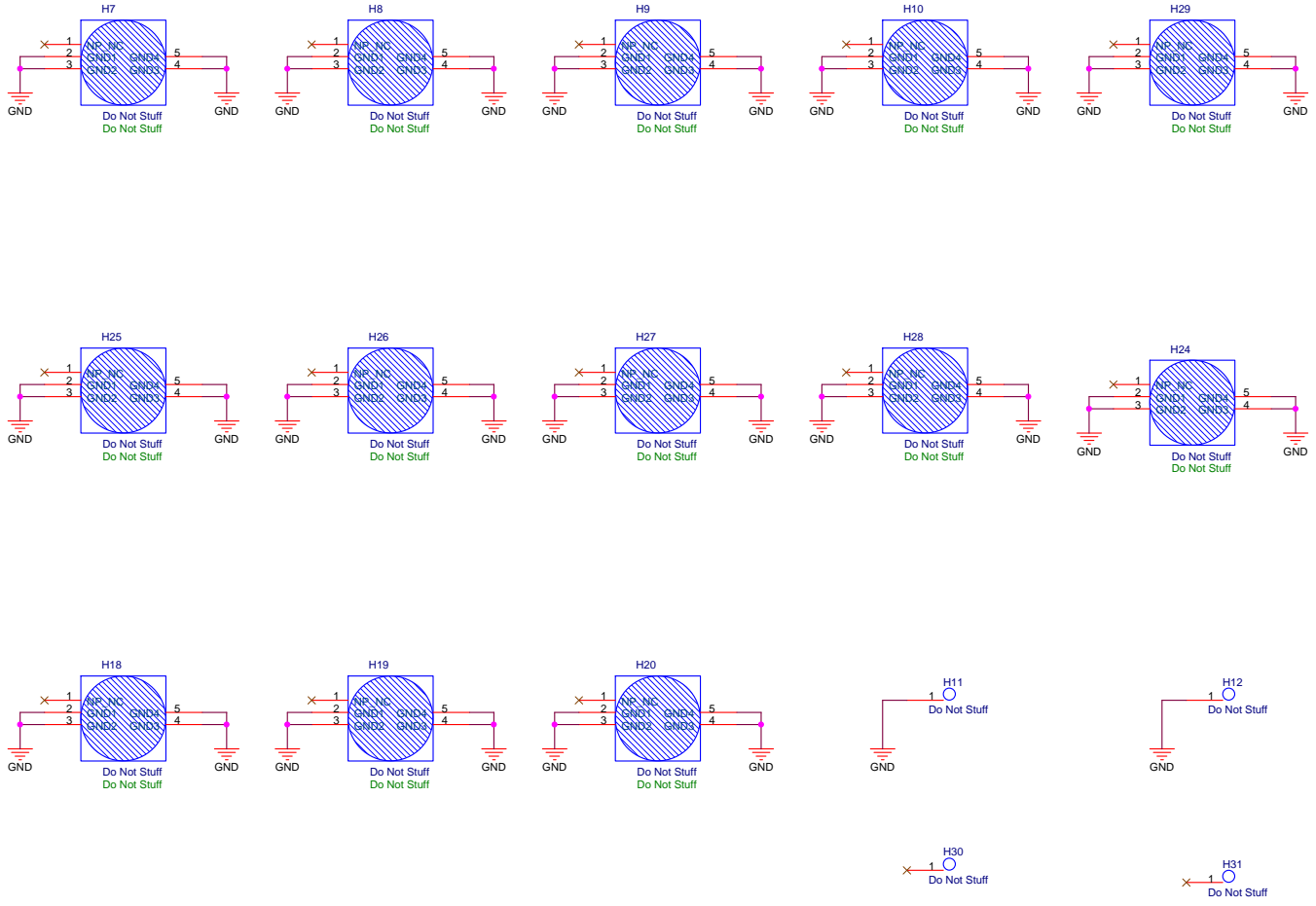
BATT_CON2



Internal BAT

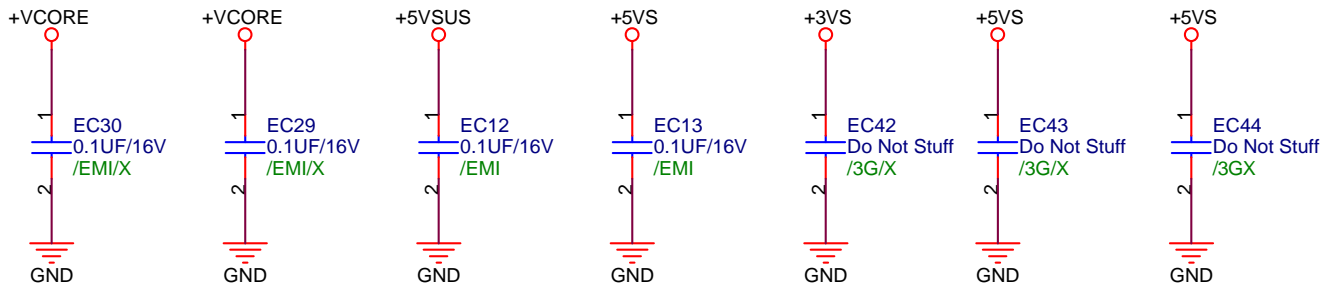
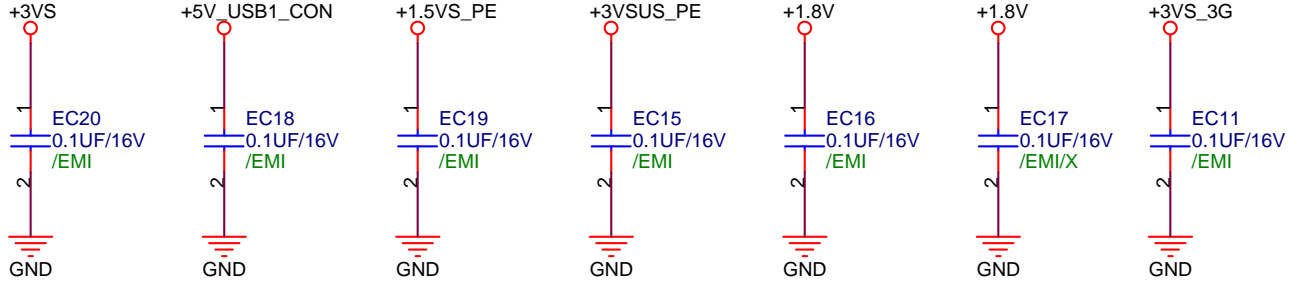
T91MT R1.0G

		Title : PWR Jack	
		ASUSTek Computer INC.	
Size		Project Name	
A4		T91MT	
Date: Tuesday, July 07, 2009		Sheet 46 of 57	



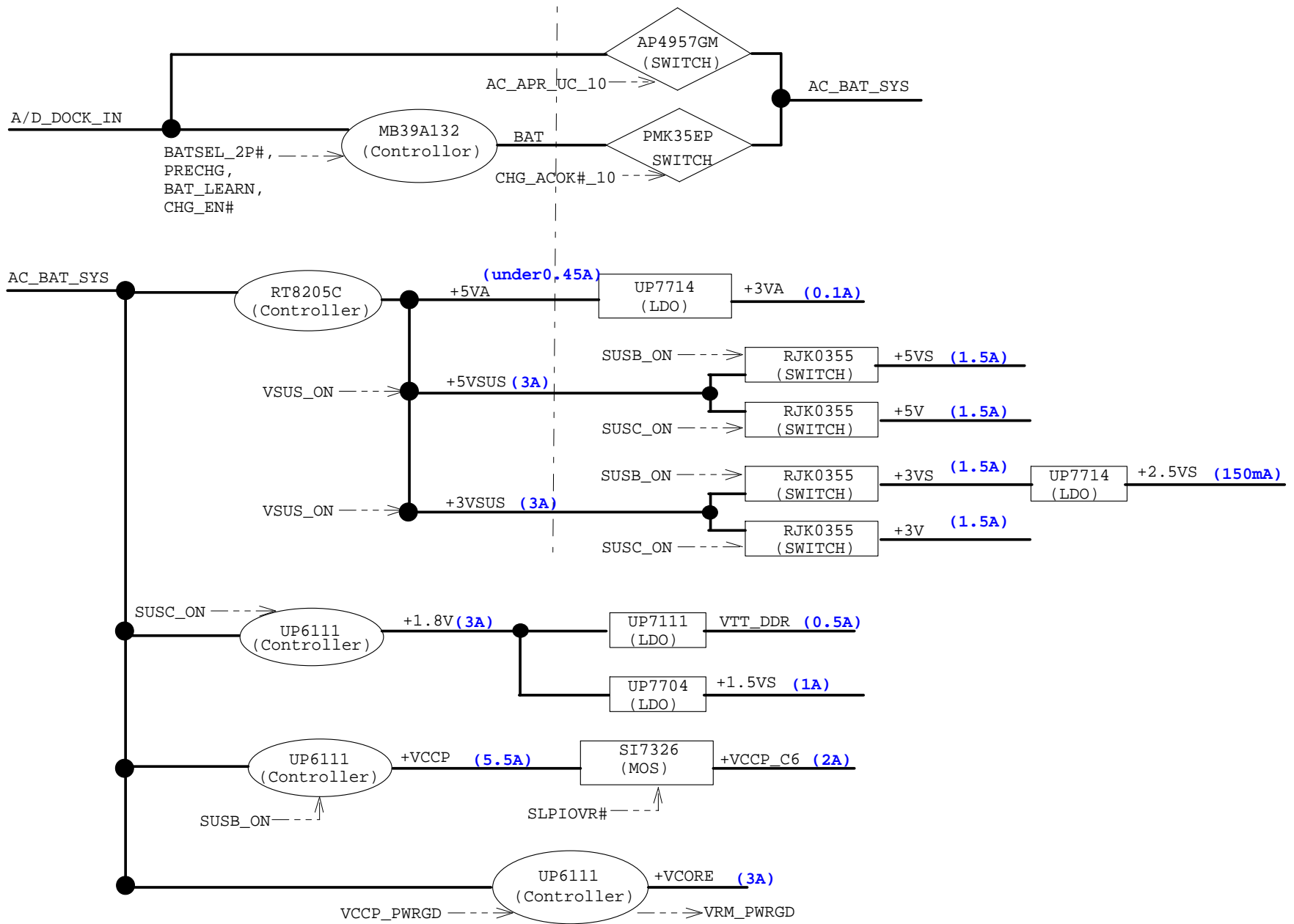
T91MT R1.0G

ASUS		Title : Screw Hole	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
A3	T91MT		
Date: Tuesday, July 07, 2009	Sheet	47	of 57



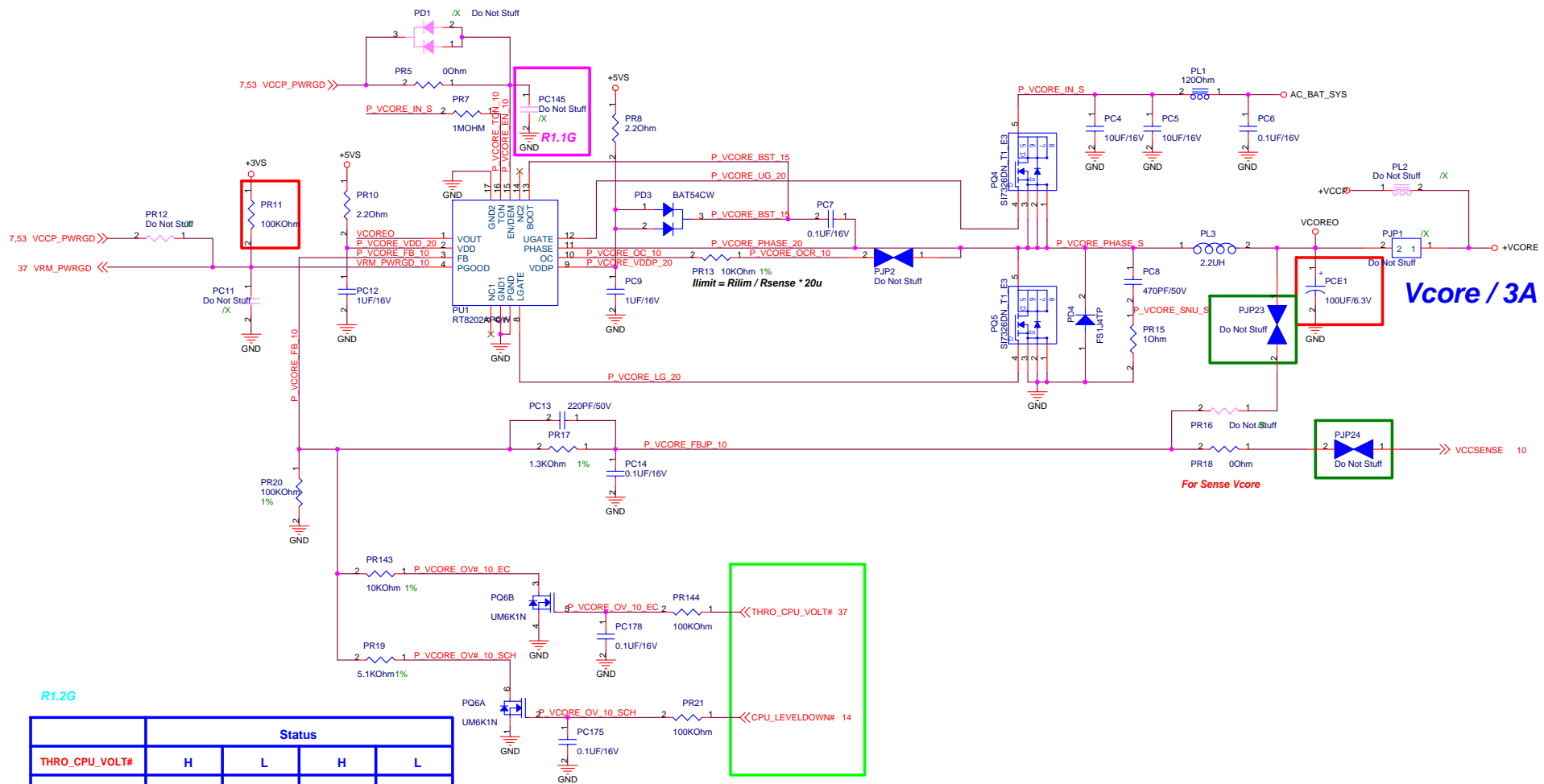
T91MT R1.0G

		Title : EMI	
ASUSTek Computer INC.		Engineer:	
Size A	Project Name T91MT		Rev
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T91MT R1.0G

ASUS		Title : Power Flow
ASUSTek Computer INC.		Engineer:
Size	Project Name	Rev
A3	T91MT	
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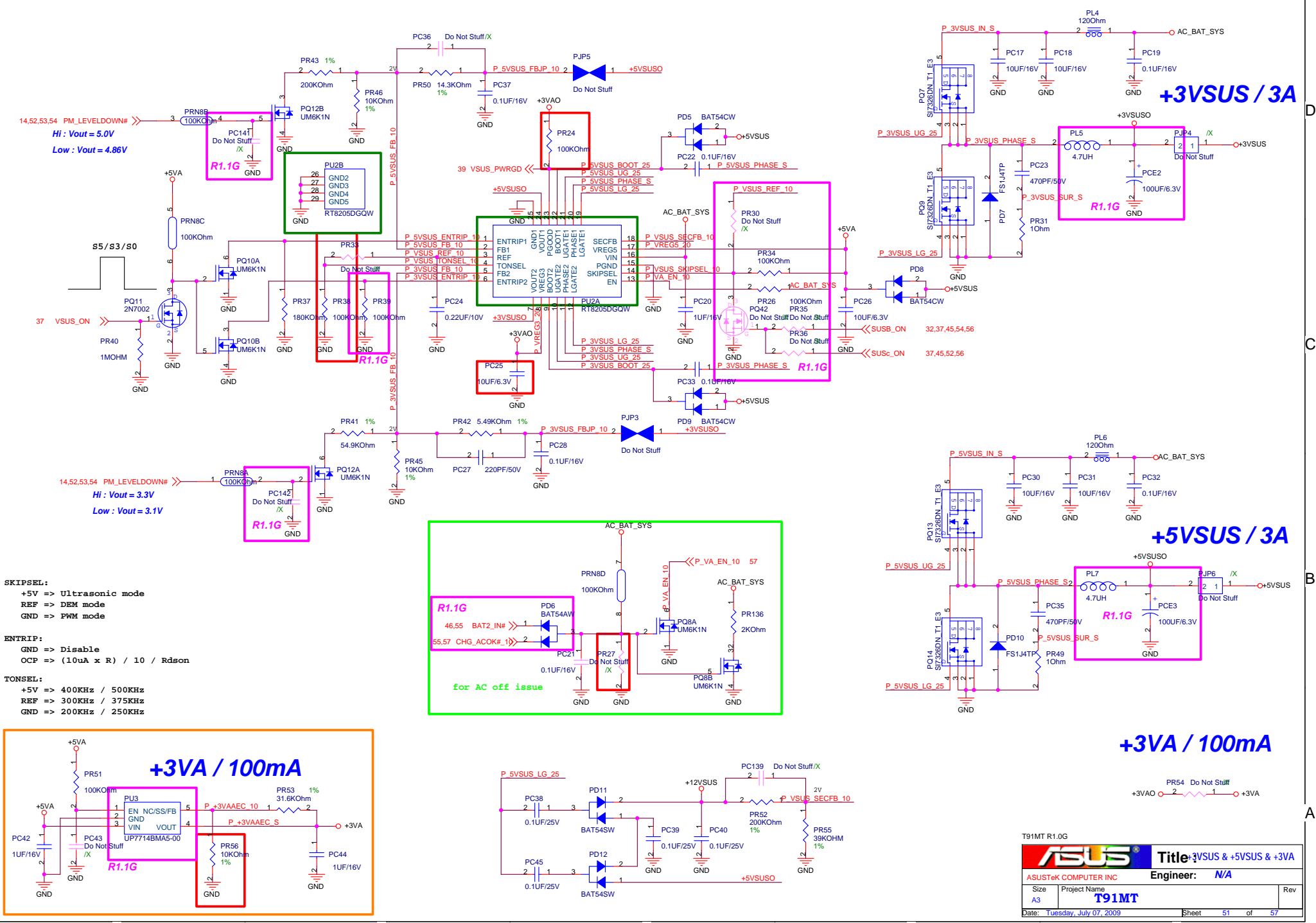


R1.2G

Status				
THRO_CPU_VOLT#	H	L	H	L
CPU_LEVELDOWN#	H	H	L	L
Voltage	1.0484V	0.9509V	0.8573V	0.7598V
	Normal	Normal + Throttle	Power Saving	Power Saving + Throttle

T91MT R1.0G

ASUS		Title : Vcore	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
Custom	T91MT		
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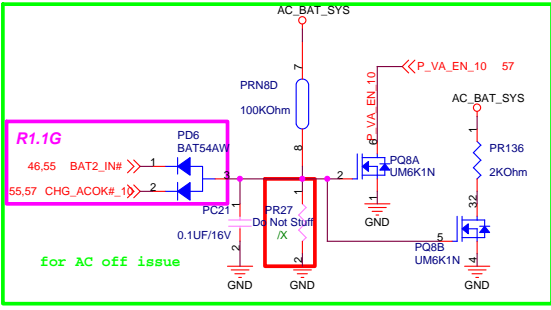
14.52.53.54 PM_LEVELDOWN#
 Hi : Vout = 5.0V
 Low : Vout = 4.86V

14.52.53.54 PM_LEVELDOWN#
 Hi : Vout = 3.3V
 Low : Vout = 3.1V

SKIPSEL:
 +5V => Ultrasonic mode
 REF => DEM mode
 GND => PWM mode

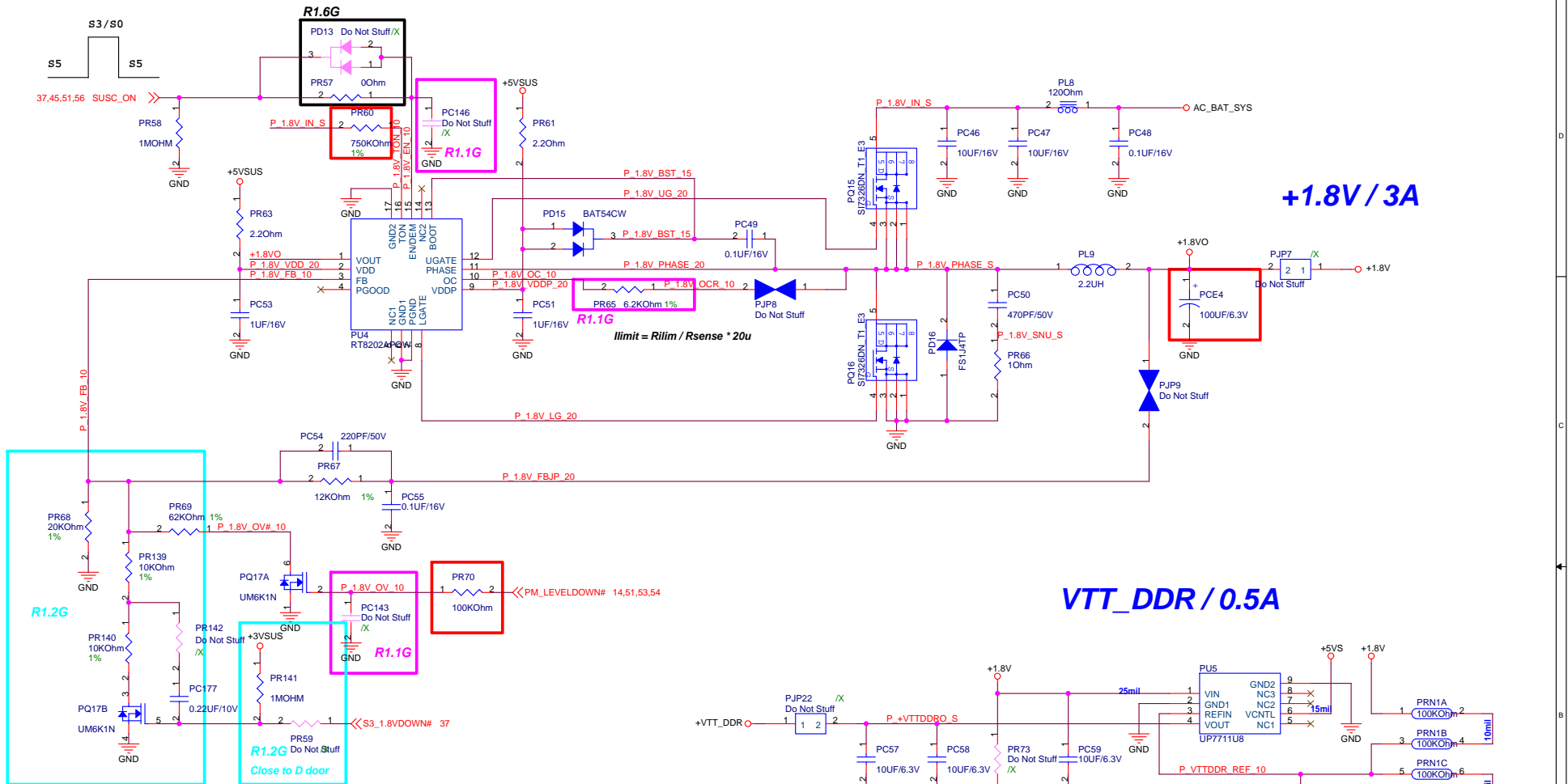
ENTRIP:
 GND => Disable
 OCP => (10uA x R) / 10 / Rds(on)

TONSEL:
 +5V => 400KHz / 500KHz
 REF => 300KHz / 375KHz
 GND => 200KHz / 250KHz



T91MT R1.0G

ASUS		Title: +3VSUS & +5VSUS & +3VA	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size A3	Project Name T91MT	Rev	
Date: Tuesday, July 07, 2009		Sheet	51 of 57



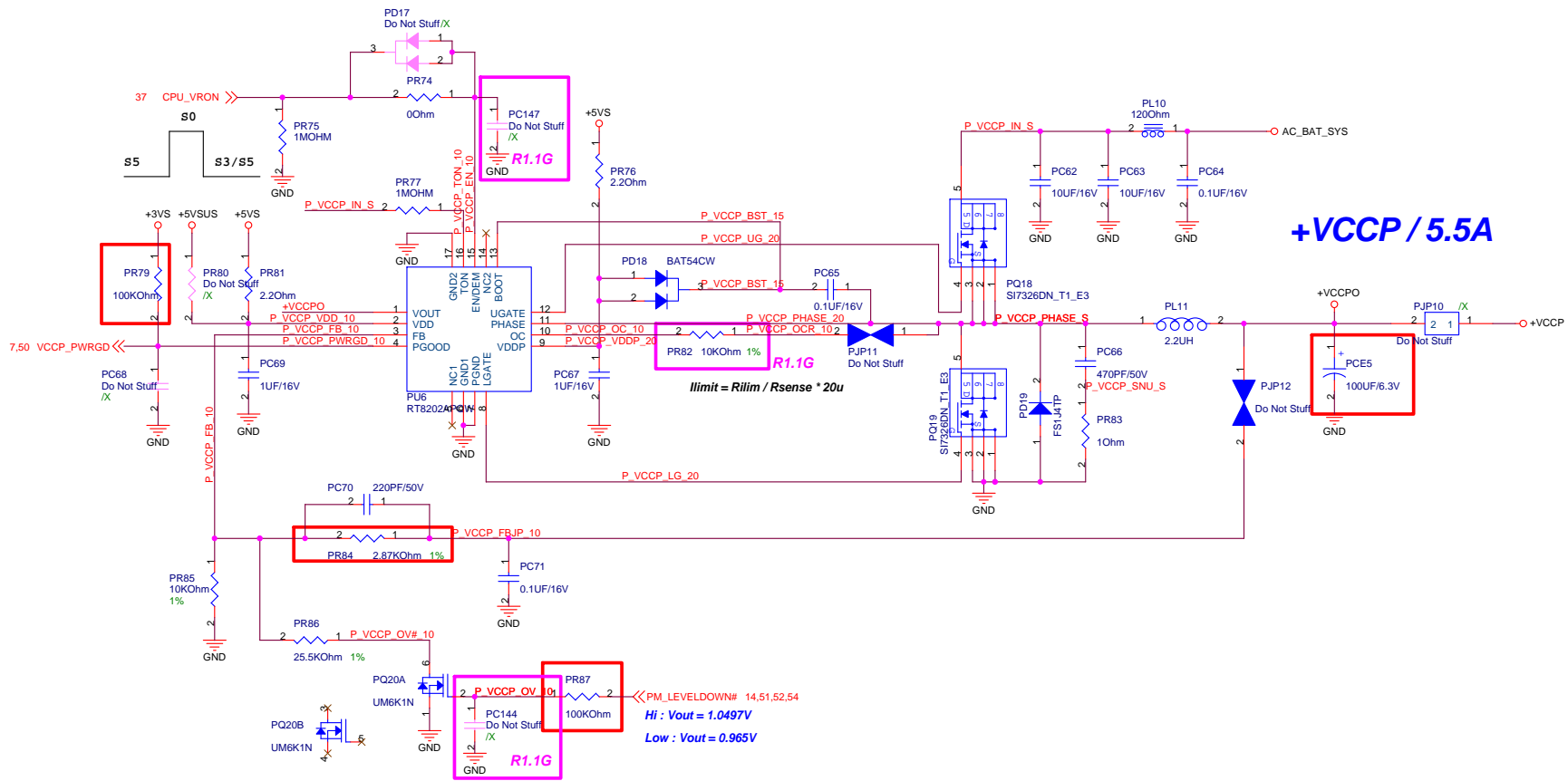
+1.8V / 3A

VTT_DDR / 0.5A

PM_LEVELDOWN#	Voltage	Status
L	1.65V	Power Saving
H	1.795V	Normal

T91MT R1.0G

		Title : +1.8V & VTTDDR
ASUSTek Computer INC.		Engineer: Joy_Zhou
Size A3	Project Name T91MT	Rev
Date: Tuesday, July 07, 2009	Sheet 52 of 57	



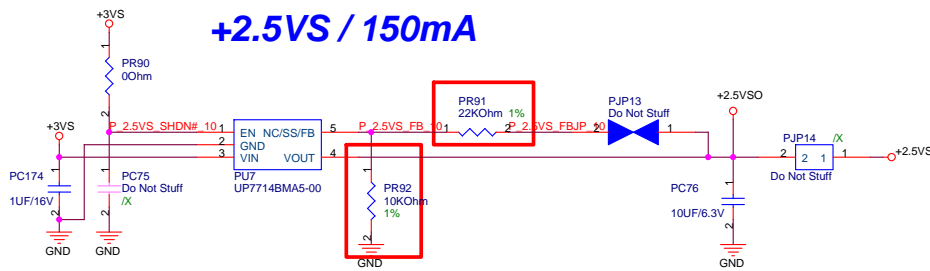
PM_LEVELDOWN#	Voltage	Status
L	0.965V	Power Saving
H	1.0497V	Normal

T91MT R1.0G

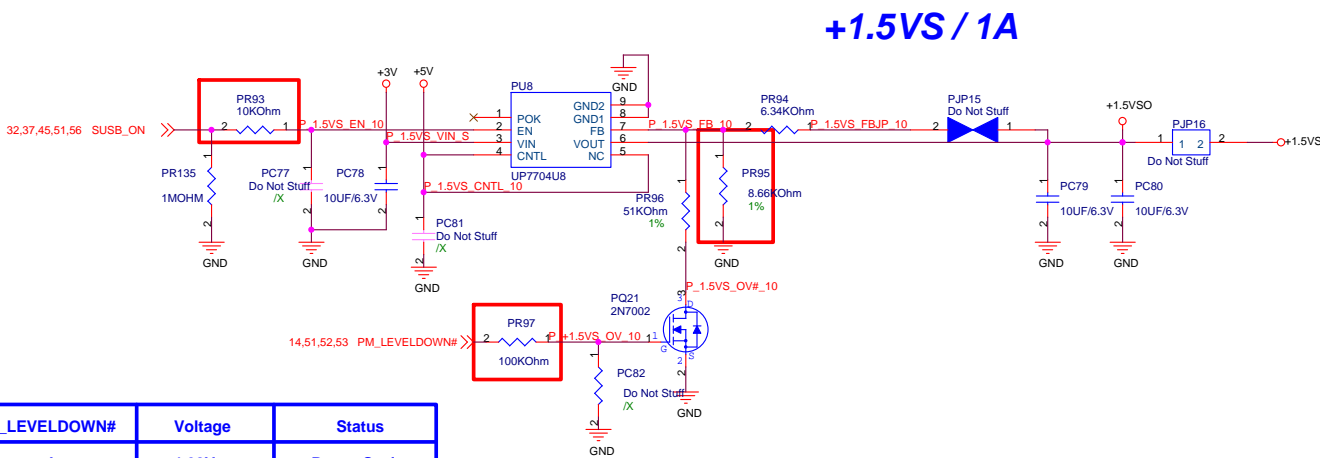
ASUS Title : VCCP
 ASUSTek Computer INC. Engineer: Joy_Zhou

Size	Project Name	Rev
A3	T91MT	

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+2.5VS / 150mA



+1.5VS / 1A

PM_LEVELDOWN#	Voltage	Status
L	1.38V	Power Saving
H	1.48V	Normal

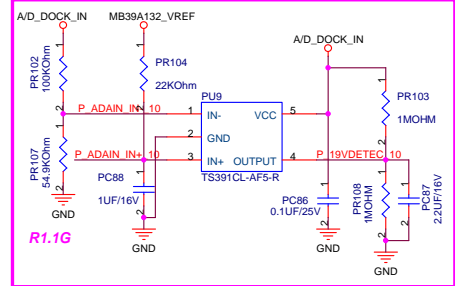
T91MT R1.0G

ASUS Title : +1.5VS & +2.5VS

ASUSTek Computer INC. Engineer: Joy_Zhou

Size	Project Name	Rev
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Prevent Input from 19V :
 Adaptor > 14.2V, PQ603B Turn-off
 Adaptor < 12.4V, PQ603B Turn-on

VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
 Soft start: $t_s(s) = 0.13 * CS (\mu F)$

VTH of -IN1: $5V / 62 * (100+62) = 13.06V$

VTH of ACIN: $1.25V / 25 * (185+25) = 10.5V$
 Change PR607 and PR608 value

Prevent Input from 19V :
 Adaptor > 13.06V, PQ603B Turn-off
 Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :
 BAT_ID = 1, 2 Cells; $V_{adj2} = 0.998V$
 $\Rightarrow I_{charge} = 1.477A$
 BAT_ID = 0, 4/6 Cells; $V_{adj2} = 1.648V$
 $\Rightarrow I_{charge} = 2.517A$

Pre-Charging Mode :
 Precharging current = 150mA
 $V_{adj2} = 168.75mV$

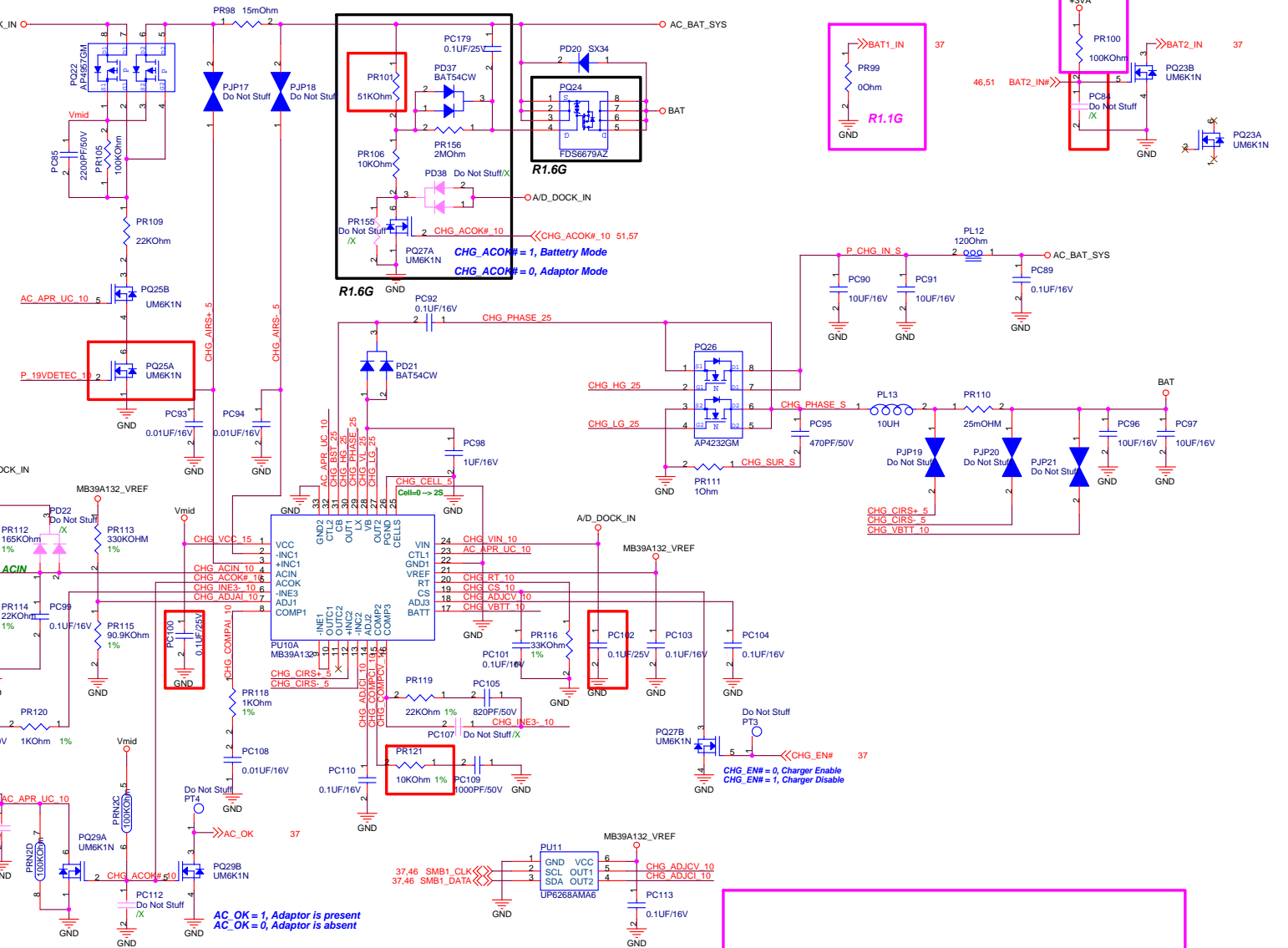
Adaptor Max. Current :
 PR600=235.8K; $I_{limit} = 2.170A$; 20.615W (9.5V/22W)
 PR600=185.3K; $I_{limit} = 2.677A$; 32.124W (12V/36W)

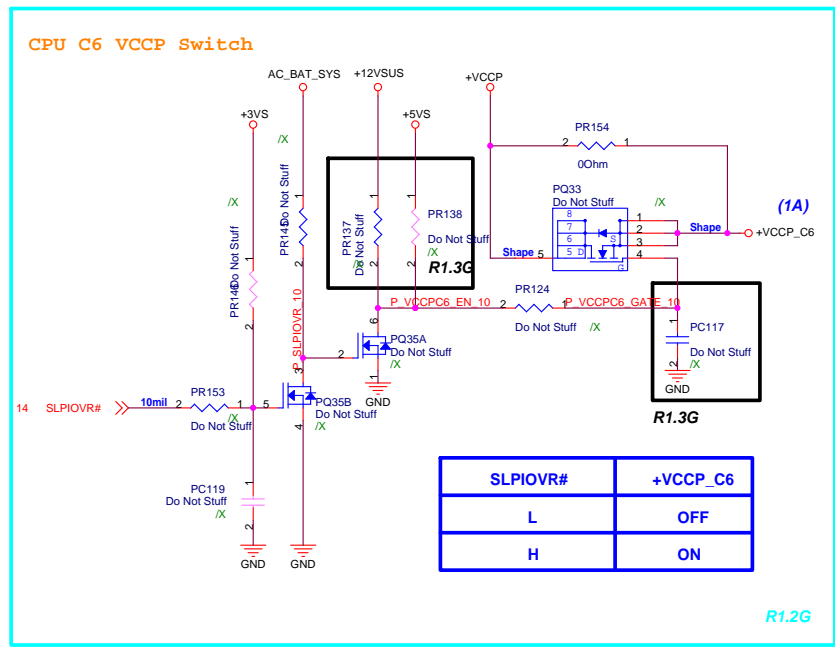
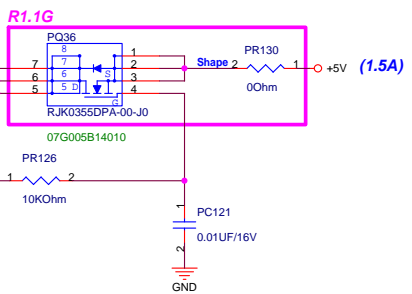
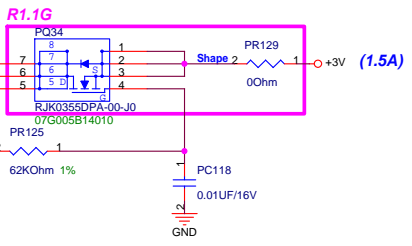
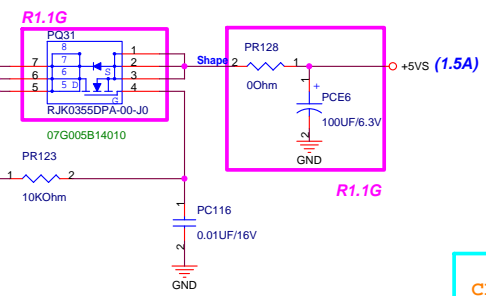
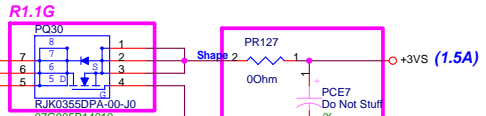
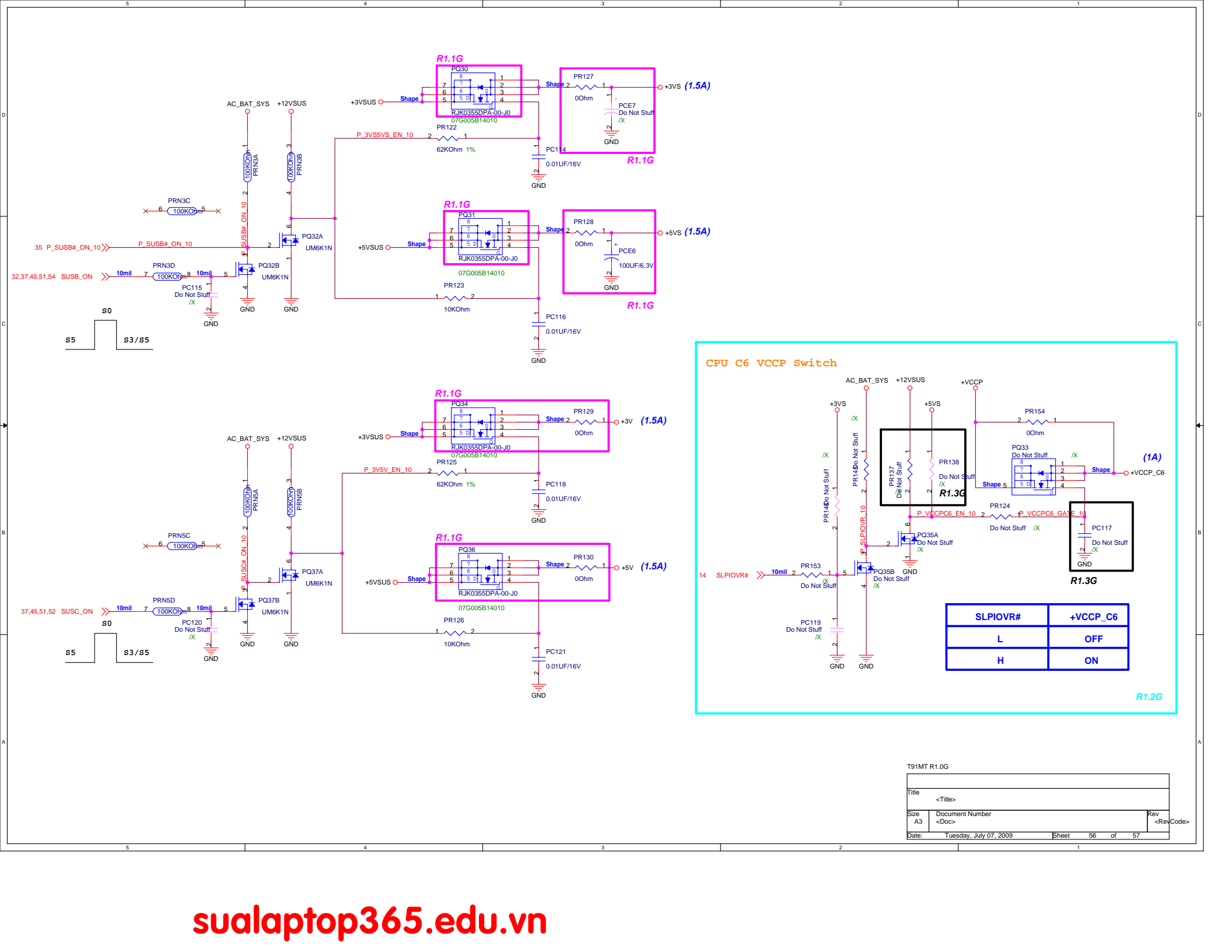
ACIN Threshold = 1.25V
 Adaptor > 10.5V, System Powered by Adaptor
 Adaptor < 10.5V, System Powered by Battery

Battery Charging Voltage :
 $V_{adj3} > 4.1V \Rightarrow V_{bat} = 4.2V / cell$
 $2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 * V_{adj3} / cell$

Battery Charging Current :
 $4.4V > V_{adj2} \geq 0V \Rightarrow$
 $I_{chg} = (V_{adj2} - 0.075) / (25 * R_s)$

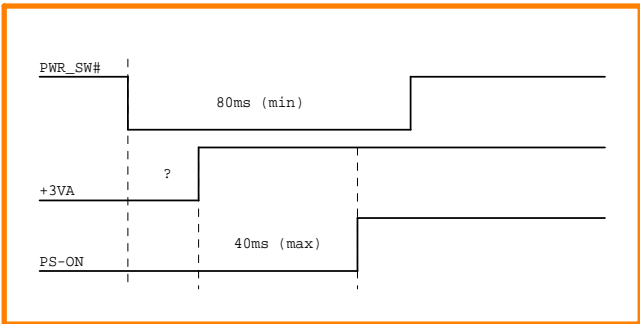
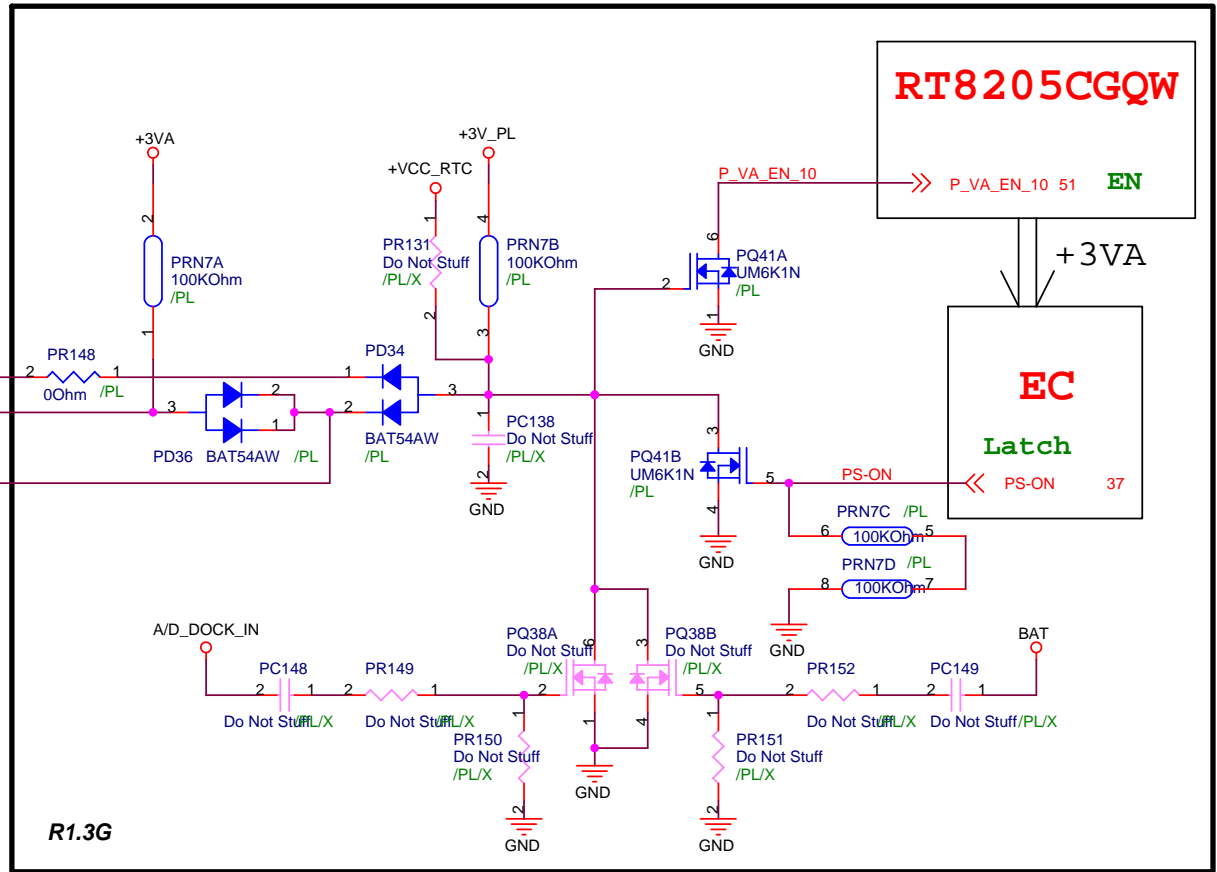
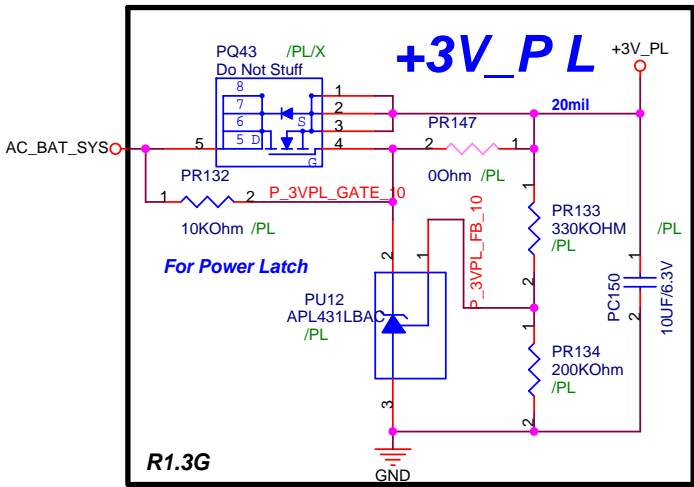
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 * R_s)$





T91MT R1.0G

Title	<Title>	
Size	Document Number	Rev
A3	<Doc>	<RevCode>
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T91MT R1.0G

		Title : Power Latch	
ASUSTek Computer INC.		Engineer: <i>Jerry Liu</i>	
Size A4	Project Name T91MT		Rev
Date: Tuesday, July 07, 2009		Sheet 57 of 57	