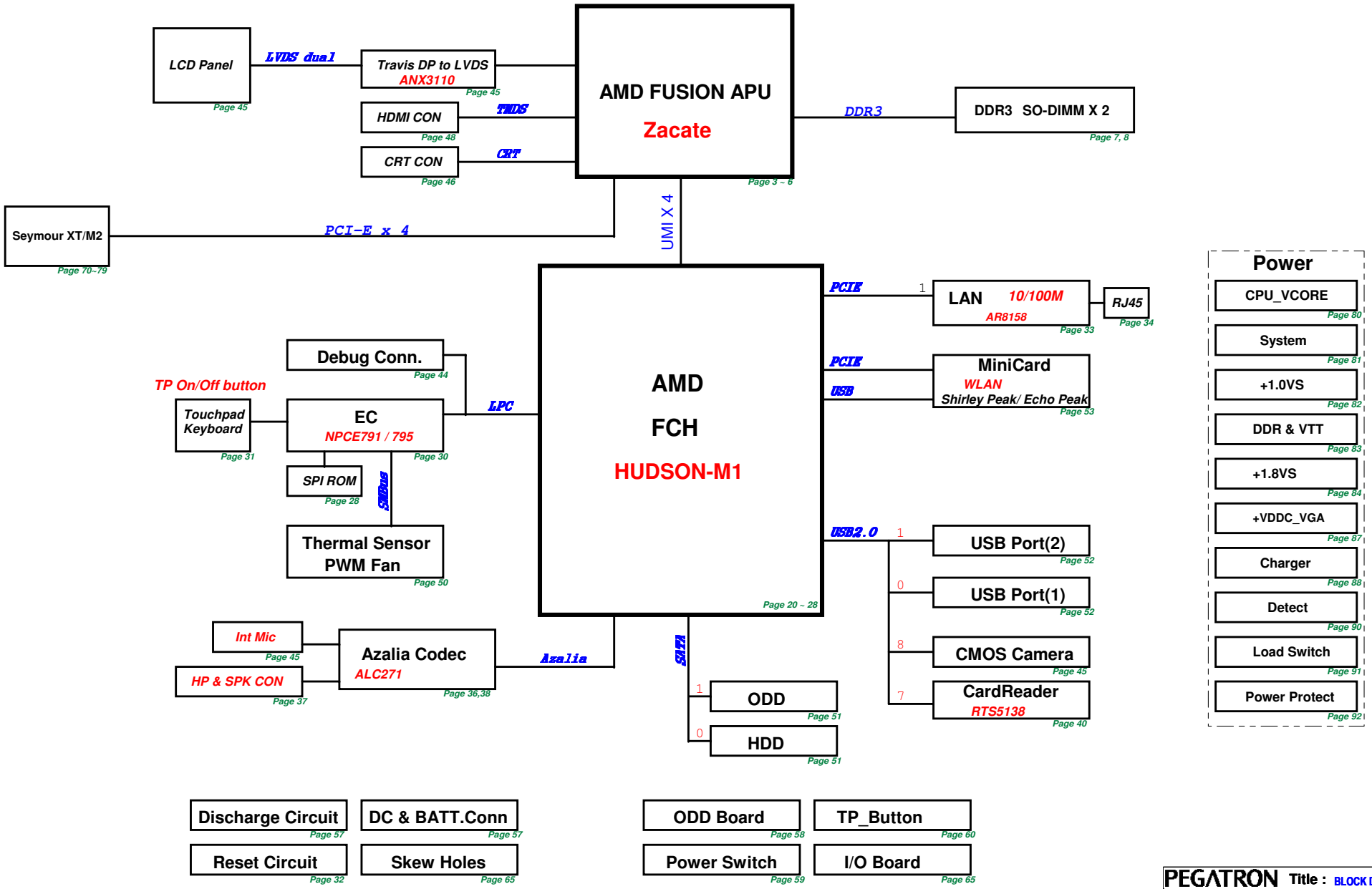
AAB70 AMD Brazos Platform Rev. 2.0

BLOCK DIAGRAM

R 1.1 /0301



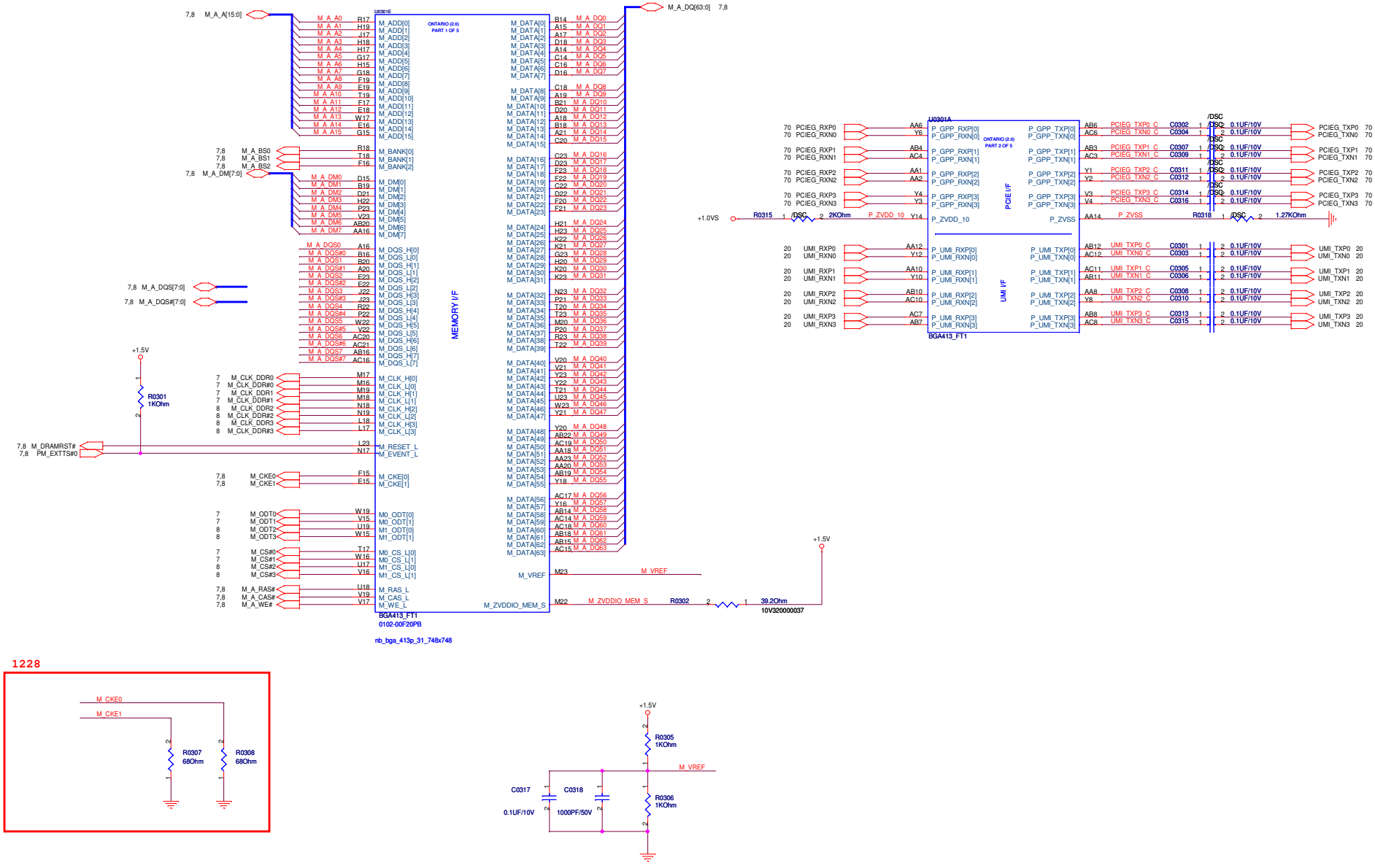
PEGATRON	Title : BLOCK DIAGRAM		
	Engineer: Allen_CD_Wu		
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 1 of 99		

PEGATRON Title : System Setting

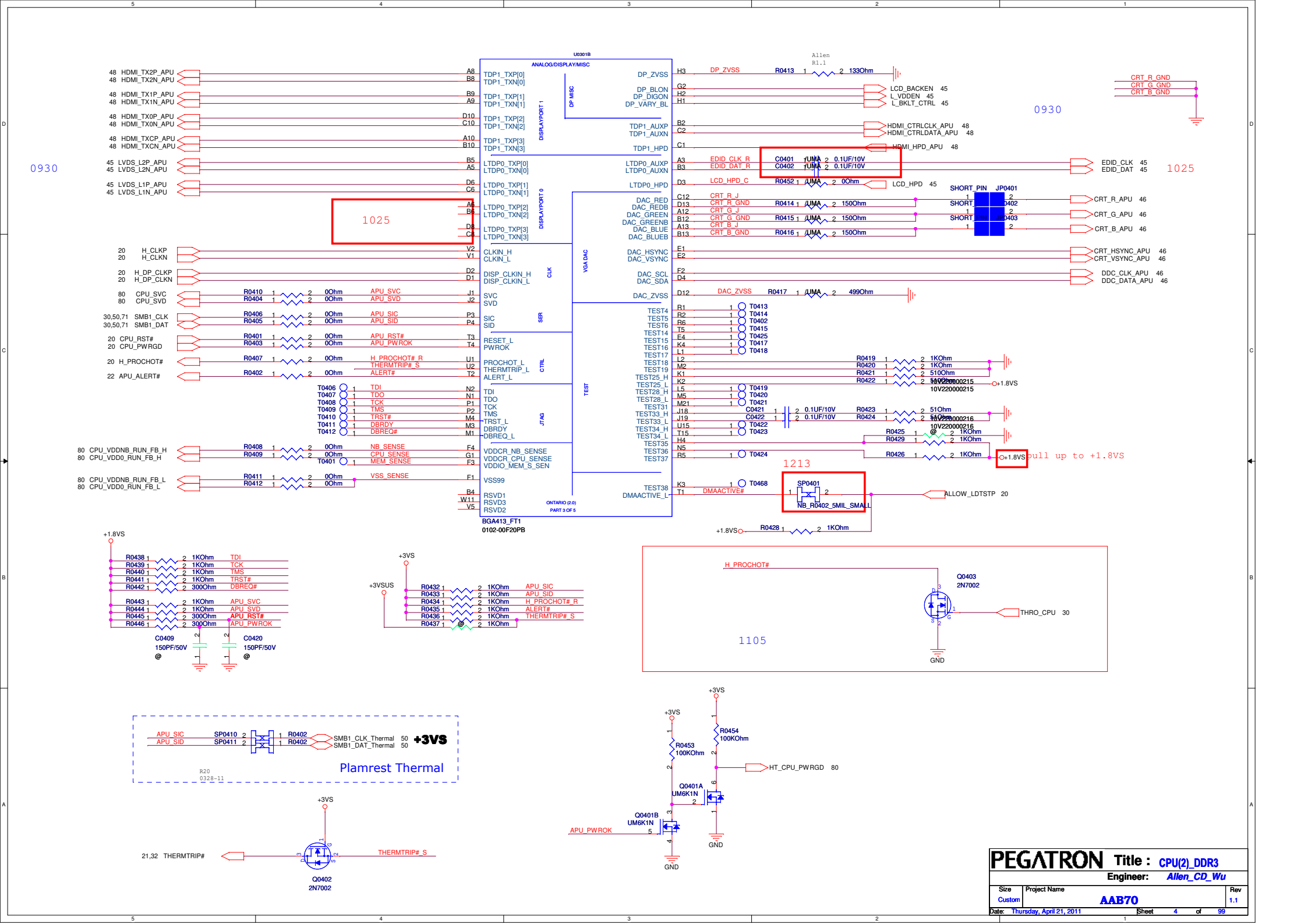
Engineer: Allen_CD_Wu

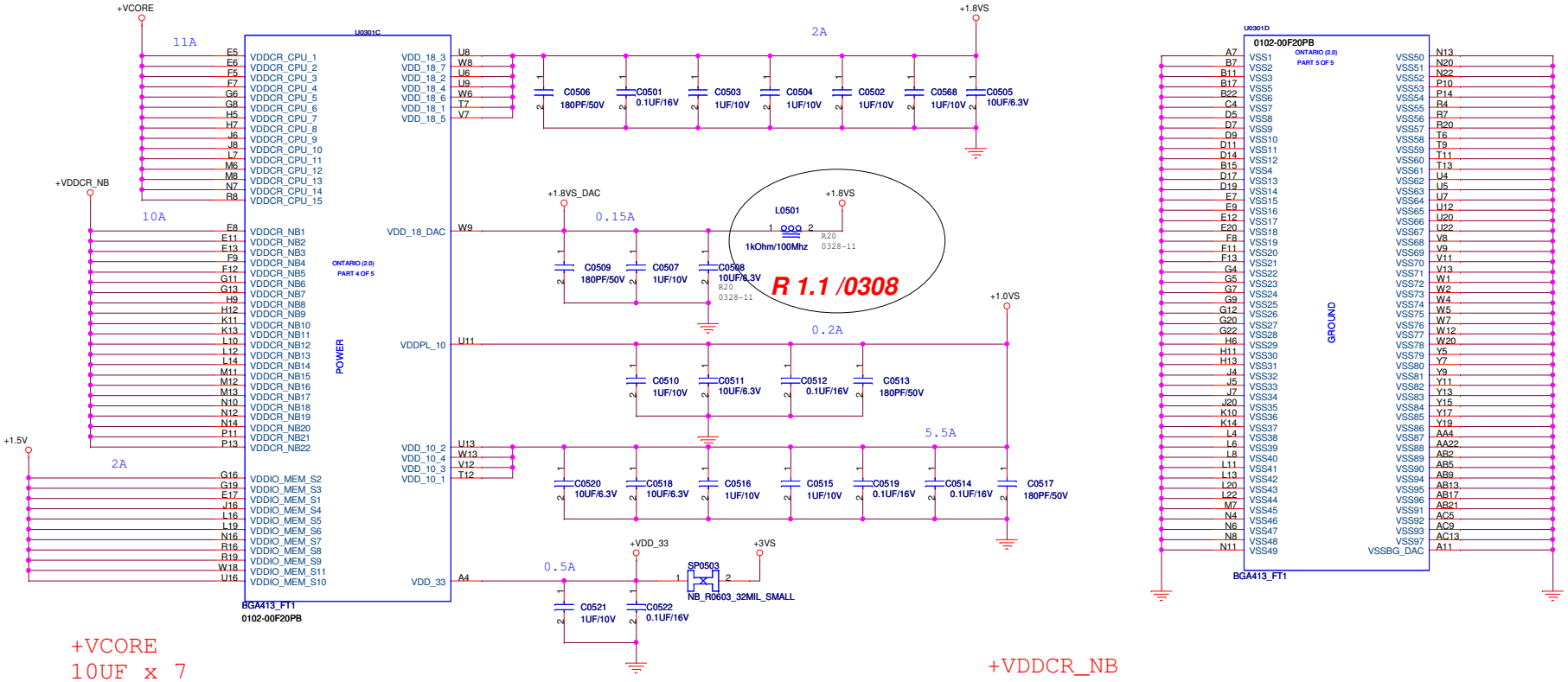
Size	Project Name	Rev
C	AAB70	1.1

Date: Monday, March 21, 2011 Sheet 2 of 99



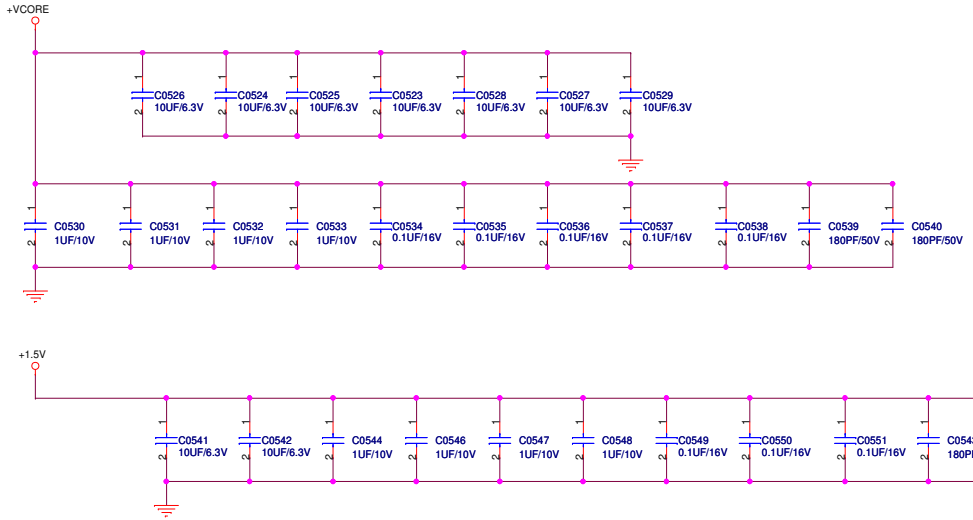
PEGATRON	Title : CPU(1)_DMI,PEG		
BG1/HW2	Engineer: Allen_CD_Wu		
Size: C	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 3 of 99		

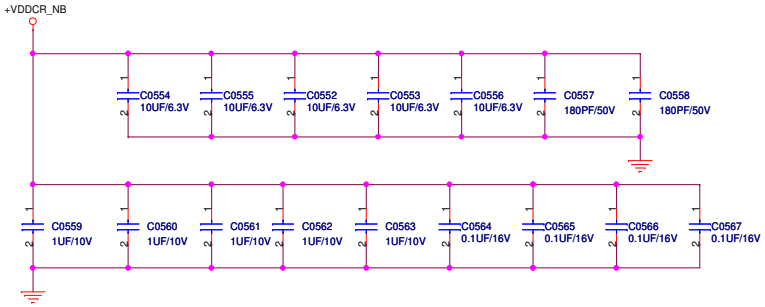

U0301B
ANALOG/DISPLAY/MISC
BGA413_FT1
0102-00F20PB
Allen
R1.1
0930
1025
1213
1105
pull up to +1.8VS
Plamrest Thermal
+3VS
Title : CPU(2)_DDR3
Engineer: Allen_CD_Wu
Project Name
AAB70
Rev
1.1
Size
Custom
Date: Thursday, April 21, 2011
Sheet 4 of 99



+VCORE
10UF x 7
1UF x 4
0.1UF x 5
180PF x 2

+VDDCR_NB
10UF x 7
1UF x 4
0.1UF x 5
180PF x 2





PEGATRON Title : CPU(3)_CFG,GND

Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

Date: Thursday, April 21, 2011 Sheet 5 of 99

PEGATRON Title : CPU(4)_PWR

Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

Date: Monday, March 21, 2011 Sheet 6 of 99

H:4.0mm 1202-002H000

R 1.1 /0308
Change PN to 8mm H

+1.5V → +1.5V_DDR3

J0701A

3,8 M_A_A[15:0]

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

3 M_CLK_DDR1 102 CK1
3 M_CLK_DDR#1 104 CK1#
3 M_CLK_DDR0 101 CK0
3 M_CLK_DDR#0 103 CK0#

3 M_CS#1 121 S1#
3 M_CS#0 114 S0#

3 M_ODT1 120 ODT1
3 M_ODT0 116 ODT0

3,8 M_A_WE# 113 WE#
3,8 M_A_RAS# 110 RAS#
3,8 M_A_CAS# 115 CAS#

3,8 M_A_BS2 79 BA2
3,8 M_A_BS1 108 BA1
3,8 M_A_BS0 109 BA0

3,8 M_CKE1 74 CKE1
3,8 M_CKE0 73 CKE0

201 SA1
197 SA0

SMBus Slave Address: A0H

3,8 M_A_DQS[7:0]
3,8 M_A_DQS#[7:0]

M_A_DQS6 188 DQS7
M_A_DQS#6 186 DQS#7
M_A_DQS7 171 DQS6
M_A_DQS#7 169 DQS#6
M_A_DQS5 154 DQS5
M_A_DQS#5 152 DQS#5
M_A_DQS4 137 DQS4
M_A_DQS#4 135 DQS#4
M_A_DQS3 64 DQS3
M_A_DQS#3 62 DQS#3
M_A_DQS2 47 DQS2
M_A_DQS#2 45 DQS#2
M_A_DQS1 29 DQS1
M_A_DQS#1 27 DQS1#
M_A_DQS0 12 DQS0
M_A_DQS#0 10 DQS0#

3,8 M_A_DM[7:0]

M_A_DM6 187 DM7
M_A_DM7 170 DM6
M_A_DM5 153 DM5
M_A_DM4 136 DM4
M_A_DM3 63 DM3
M_A_DM2 46 DM2
M_A_DM1 28 DM1
M_A_DM0 11 DM0

8,21 SMB_CLK_S 202 SCL
8,21 SMB_DAT_S 200 SDA

RESET# 30 M_DRAMRST# 3,8

M_A_DQ[63:0] 3,8

DQ0 5 M_A_DQ7
DQ1 7 M_A_DQ2
DQ2 15 M_A_DQ4
DQ3 17 M_A_DQ5
DQ4 4 M_A_DQ3
DQ5 6 M_A_DQ6
DQ6 16 M_A_DQ1
DQ7 18 M_A_DQ0
DQ8 21 M_A_DQ12
DQ9 23 M_A_DQ13
DQ10 33 M_A_DQ15
DQ11 35 M_A_DQ14
DQ12 22 M_A_DQ8
DQ13 24 M_A_DQ9
DQ14 34 M_A_DQ11
DQ15 36 M_A_DQ10
DQ16 39 M_A_DQ21
DQ17 41 M_A_DQ20
DQ18 51 M_A_DQ22
DQ19 53 M_A_DQ19
DQ20 40 M_A_DQ17
DQ21 42 M_A_DQ16
DQ22 50 M_A_DQ23
DQ23 52 M_A_DQ18
DQ24 57 M_A_DQ28
DQ25 59 M_A_DQ29
DQ26 67 M_A_DQ31
DQ27 69 M_A_DQ26
DQ28 56 M_A_DQ25
DQ29 58 M_A_DQ24
DQ30 68 M_A_DQ30
DQ31 70 M_A_DQ27
DQ32 129 M_A_DQ33
DQ33 131 M_A_DQ32
DQ34 141 M_A_DQ39
DQ35 143 M_A_DQ35
DQ36 130 M_A_DQ37
DQ37 132 M_A_DQ36
DQ38 140 M_A_DQ38
DQ39 142 M_A_DQ34
DQ40 147 M_A_DQ41
DQ41 149 M_A_DQ40
DQ42 157 M_A_DQ46
DQ43 159 M_A_DQ47
DQ44 146 M_A_DQ45
DQ45 148 M_A_DQ44
DQ46 158 M_A_DQ42
DQ47 160 M_A_DQ43
DQ48 163 M_A_DQ56
DQ49 165 M_A_DQ61
DQ50 175 M_A_DQ63
DQ51 177 M_A_DQ59
DQ52 164 M_A_DQ60
DQ53 166 M_A_DQ57
DQ54 174 M_A_DQ58
DQ55 176 M_A_DQ62
DQ56 181 M_A_DQ49
DQ57 183 M_A_DQ53
DQ58 191 M_A_DQ55
DQ59 193 M_A_DQ54
DQ60 180 M_A_DQ48
DQ61 182 M_A_DQ52
DQ62 192 M_A_DQ50
DQ63 194 M_A_DQ51

0 1 2 3 4 5 6 7

DDR3_DIMM_204P
12V02GIRM001

1006

EMI request

+1.5V_DDR3
C0722 0.1UF/16V
C0723 0.1UF/16V
C0724 0.1UF/16V
C0725 0.1UF/16V

+1.5V_DDR3
Layout Note: Place these caps near SO DIMM 0

C0705 10UF/6.3V @
C0706 10UF/6.3V
C0707 10UF/6.3V
C0708 10UF/6.3V
C0709 10UF/6.3V
C0710 10UF/6.3V

+1.5V_DDR3
Layout Note: Place these caps near SODIMM 0

C0701 0.1UF/10V
C0702 0.1UF/10V
C0703 0.1UF/10V
C0704 0.1UF/10V

J0701B

VDD1 75 VDD2 76
VDD3 81 VDD4 82
VDD5 87 VDD6 88
VDD7 93 VDD8 94
VDD9 99 VDD10 100
VDD11 105 VDD12 106
VDD13 111 VDD14 112
VDD15 117 VDD16 118
VDD17 123 VDD18 124

VSS1 2 VSS2 3
VSS3 8 VSS4 9
VSS5 13 VSS6 14
VSS7 19 VSS8 20
VSS9 25 VSS10 26
VSS11 31 VSS12 32
VSS13 37 VSS14 38
VSS15 43 VSS16 44
VSS17 48 VSS18 49
VSS19 54 VSS20 55
VSS21 60 VSS22 61
VSS23 65 VSS24 66
VSS25 71 VSS26 72
VSS27 127 VSS28 128
VSS29 133 VSS30 134
VSS31 138 VSS32 139
VSS33 144 VSS34 145
VSS35 150 VSS36 151
VSS37 155 VSS38 156
VSS39 161 VSS40 162
VSS41 167 VSS42 168
VSS43 172 VSS44 173
VSS45 178 VSS46 179
VSS47 184 VSS48 185
VSS49 189 VSS50 190
VSS51 195 VSS52 196

GND1 207
GND2 208

3,8 PM_EXTTS#0 R0701 2 @ 1 0Ohm DIM_EXTTS#0 198 EVENT#
TEST 125
NC1 77
NC2 122
NP_NC1 205
NP_NC2 206
VTT1 203 +0.75VS
VTT2 204
VREFCA 126
VREFDQ 1
VDDSPD 199 +3VS

DDR3_DIMM_204P
12V02GIRM001

M_VREFDQ_DIMM0
C0711 1000PF/50V
C0712 0.1UF/10V

M_VREFDQ_DIMM0
C0713 1000PF/50V
C0714 0.1UF/10V

C0715 0.1UF/10V
C0716 2.2UF/10V

0301
1202-00E1000-->12V02GIRM001

+0.75VS
C0720 1UF/6.3V @
C0717 1UF/6.3V
C0718 1UF/6.3V
C0719 1UF/6.3V

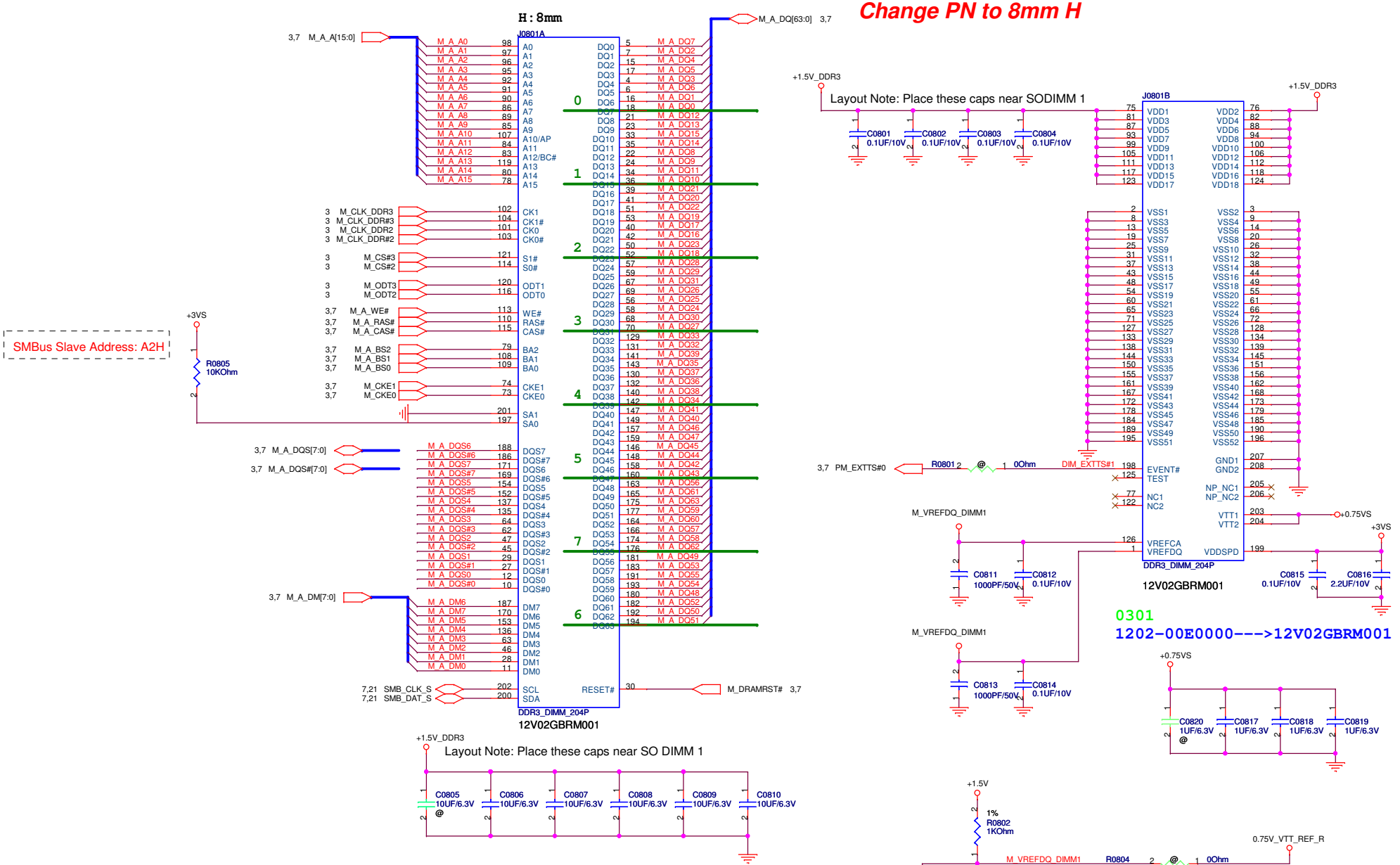
+1.5V
1% R0702 1KOhm
M_VREFDQ_DIMM0 R0704 2 @ 1 0Ohm 0.75V_VTT_REF_R
C0721 0.1UF/10V
1% R0703 1KOhm

PEGATRON	Title : DDR3(1)_SO-DIMM0	
	Engineer: Allen_CD_Wu	
Size: Custom	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 7 of 99	

H:8.0mm 1202-000P000

R 1.1 /0308
Change PN to 8mm H

H : 8mm



PEGATRON	Title : DDR3(2)_SO-DIMM1		
	Engineer: Allen_CD_Wu		
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011		Sheet 8 of 99	

PEGATRON Title : DDR3(3)_CA/DQ Voltage

Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

Date: Monday, March 21, 2011 Sheet 9 of 99

HUDSON-1

U2001E

PCIERST# / A_RST#

UMI_RXP0 C2001 0.1UF/10V UMI_RXP0_C AD26
UMI_RXN0 C2002 0.1UF/10V UMI_RXN0_C AD27
UMI_RXP1 C2003 0.1UF/10V UMI_RXP1_C AC28
UMI_RXN1 C2004 0.1UF/10V UMI_RXN1_C AC29
UMI_RXP2 C2005 0.1UF/10V UMI_RXP2_C AB29
UMI_RXN2 C2006 0.1UF/10V UMI_RXN2_C AB28
UMI_RXP3 C2007 0.1UF/10V UMI_RXP3_C AB26
UMI_RXN3 C2008 0.1UF/10V UMI_RXN3_C AB27

UMI_TXP0 AE24
UMI_TXN0 AE23
UMI_TXP1 AD25
UMI_TXN1 AD24
UMI_TXP2 AC24
UMI_TXN2 AC25
UMI_TXP3 AB25
UMI_TXN3 AB24

1014 PCIE_VDDR R2016 1% 590OHM PCIE_CALRP AD29
R2008 1% 2KOhm PCIE_CALRN AD28
10V320000040

C2009 0.1UF/10V PCIE_TXP1_WLAN_C AA28
C2010 0.1UF/10V PCIE_TXN1_WLAN_C AA29
C2011 0.1UF/10V PCIE_TXP2_LAN_C Y28
C2012 0.1UF/10V PCIE_TXN2_LAN_C Y26
GPP_TX3P Y27
GPP_TX3N W28
W29

GPP_RX0P AA22
GPP_RX0N Y21
GPP_RX1P AA25
GPP_RX1N AA24
GPP_RX2P W23
GPP_RX2N V24
GPP_RX3P W24
GPP_RX3N W25

PCI EXPRESS I/F

For internal clock generator mode:
NB_LNK_CLKP. Not used. Left unconnected

PCIE_RCLKP/NB_LNK_CLKP M23
PCIE_RCLKN/NB_LNK_CLKN P23
NB_DISP_CLKP U29
NB_DISP_CLKN U28
NB_HT_CLKP T26
NB_HT_CLKN T27
CPU_HT_CLKP V21
CPU_HT_CLKN T21
SLT_GFX_CLKP Y23
SLT_GFX_CLKN T23
GPP_CLK0P L29
GPP_CLK0N L28
GPP_CLK1P N29
GPP_CLK1N N28
GPP_CLK2P M29
GPP_CLK2N M28
GPP_CLK3P T25
GPP_CLK3N V25
GPP_CLK4P L24
GPP_CLK4N L23
GPP_CLK5P P25
GPP_CLK5N M25
GPP_CLK6P P29
GPP_CLK6N P28
GPP_CLK7P N26
GPP_CLK7N N27
GPP_CLK8P T29
GPP_CLK8N T28
14M_25M_48M_OSC L25
25M_X1 L26
25M_X2 L27

CLOCK GENERATOR

0929
RN2001B 4 0Ohm 3 H_DP_CLKP_R U29
RN2001A 4 0Ohm 1 H_DP_CLKN_R U28
RN2007B 4 0Ohm 3 /UMA CLK_DP_P_R T26
RN2007A 2 0Ohm 1 /UMA CLK_DP_N_R T27
RN2002A 2 0Ohm 1 H_CLKP_R V21
RN2002B 4 0Ohm 3 H_CLKN_R T21
RN2003A 2 0Ohm 1 /DSC CLK_PCIE_VGA_P_R V23
RN2003B 4 0Ohm 3 /DSC CLK_PCIE_VGA_N_R T23
RN2004A 2 0Ohm 1 CLK_PCIE_WLAN_P_R N29
RN2004B 4 0Ohm 3 CLK_PCIE_WLAN_N_R N28
RN2005A 2 0Ohm 1 CLK_PCIE_LAN_P_R M29
RN2005B 4 0Ohm 3 CLK_PCIE_LAN_N_R M28

AAB70_0125
T2008 CLK_25M_LAN
for EMI C2026 0.1UF/10V @

1213
C2015 15PF/50V
X2002 25MHZ
C2016 15PF/50V
R2021 2.2KOhm
R2011 1MOhm
X1_25M
X2_25M
GND

HUDSON-M1
0205-004J0PB

PCICLK0 W2 PCICLK0 22Ohm R2007 CLK_DEBUG 44
PCICLK1/GPO36 W1 PCICLK1 PCICLK1 24
PCICLK2/GPO37 W3 PCICLK2 PCICLK2 24
PCICLK3/GPO38 W4 PCICLK3 PCICLK3 24
PCICLK4/14M_OSC/GPO39 Y1 PCICLK4 PCICLK4 24
PCI CLKS
C2025 150PF/50V @
PCIRST# V2 PCI_RST# T2004
DGPU_HOLD_RST# T2005

AD0/GPIO0 AA1
AD1/GPIO1 AA4
AD2/GPIO2 AA3
AD3/GPIO3 AB1
AD4/GPIO4 AA5
AD5/GPIO5 AB2
AD6/GPIO6 AB6
AD7/GPIO7 AB5
AD8/GPIO8 AA6
AD9/GPIO9 AC2
AD10/GPIO10 AC3
AD11/GPIO11 AC4
AD12/GPIO12 AC1
AD13/GPIO13 AD1
AD14/GPIO14 AD2
AD15/GPIO15 AC6
AD16/GPIO16 AE2
AD17/GPIO17 AE1
AD18/GPIO18 AF8
AD19/GPIO19 AE3
AD20/GPIO20 AF1
AD21/GPIO21 AG1
AD22/GPIO22 AF2
AD23/GPIO23 AE9
AD24/GPIO24 AD9
AD25/GPIO25 AC11
AD26/GPIO26 AF6
AD27/GPIO27 AF4
AD28/GPIO28 AF3
AD29/GPIO29 AH2
AD30/GPIO30 AG2
AD31/GPIO31 AH3
CBE0# AA8
CBE1# AD5
CBE2# AD8
CBE3# AA10
FRAME# AE8
DEVSEL# AB9
IRDY# AJ3
TRDY# AE7
PAR AC5
STOP# AF5
PERR# AE6
SERR# AE4
REQ0# AE11
REQ1#/GPIO40 AH5
REQ2#/CLK_REQ8#/GPIO41 AH4
REQ3#/CLK_REQ5#/GPIO42 AC12
GNT0# AD12
GNT1#/GPO44 AJ5
GNT2#/GPO45 AH6
GNT3#/CLK_REQ7#/GPIO46 AB12
CLKRUN# AB11
LOCK# AD7
INTE#/GPIO32 AJ6
INTF#/GPIO33 AG6
INTG#/GPIO34 AG4
INTH#/GPIO35 AJ4
PCI I/F

T2006 0930
PE_GPIO1 R2005 0Ohm VGA_PWRON 75,91
T2007 R2002 0Ohm PM_CLKRUN# 30
PE_GPIO0

remove ?
AD23 24
AD24 24
AD25 24
AD26 24
AD27 24

Hudson-M1 not support PCI

LPCCLK0 H24 LPCCLK0 R2010 22Ohm CLK_KBCPCI 24,30
LPCCLK1 H25 LPCCLK1_R R2020 22Ohm LPCCLK1 24
LAD0 J27 LPC_AD0 30,44
LAD1 J26 LPC_AD1 30,44
LAD2 H29 LPC_AD2 30,44
LAD3 H28 LPC_AD3 30,44
LFRAME# G28 LPC_FRAME# 30,44
LDRQ0# J25
LDRQ1#/CLK_REQ6#/GPIO43 AA18
SERIRQ/GPIO48 AB19 INT_SERIRQ 30
LPC

ALLOW_LDTSTP/DMA_ACTIVE# G21 ALLOW_LDTSTP 4
PROCHOT# H21 R2003 0Ohm H_PROCHOT# 4
LDT_PG K19 CPU_PWRGD CPU_PWRGD 4
LDT_STP# G22
LDT_RST# J24 CPU_RST# CPU_RST# 4
CPU

32K_X1 C1 X1_RTC
32K_X2 C2 X2_RTC_R
RTCCLK D2 R2006 0Ohm RTCCLK 30
INTRUDER_ALERT# B2 R2017 1MOhm
VDDBT_RTC_G B1 R2012 0Ohm
RTC

0929
+VCC_RTC
R2013 20MOhm 10V240000043
R2019 0Ohm
X2001 32.768KHZ
C2018 22PF/50V
C2019 22PF/50V
X2_RTC
JRST2001 SGL_JUMP @

1213

BATT_HOLDER
+RTCBAT
1221 R2014 510Ohm
BAT2001 BATT_HOLDER_2P

aab70_0120
+3VA @
D2001 1V/0.2A
R2015 0Ohm
C2017 1UF/10V

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

PCIE_ARST# is for PCIE device in APU

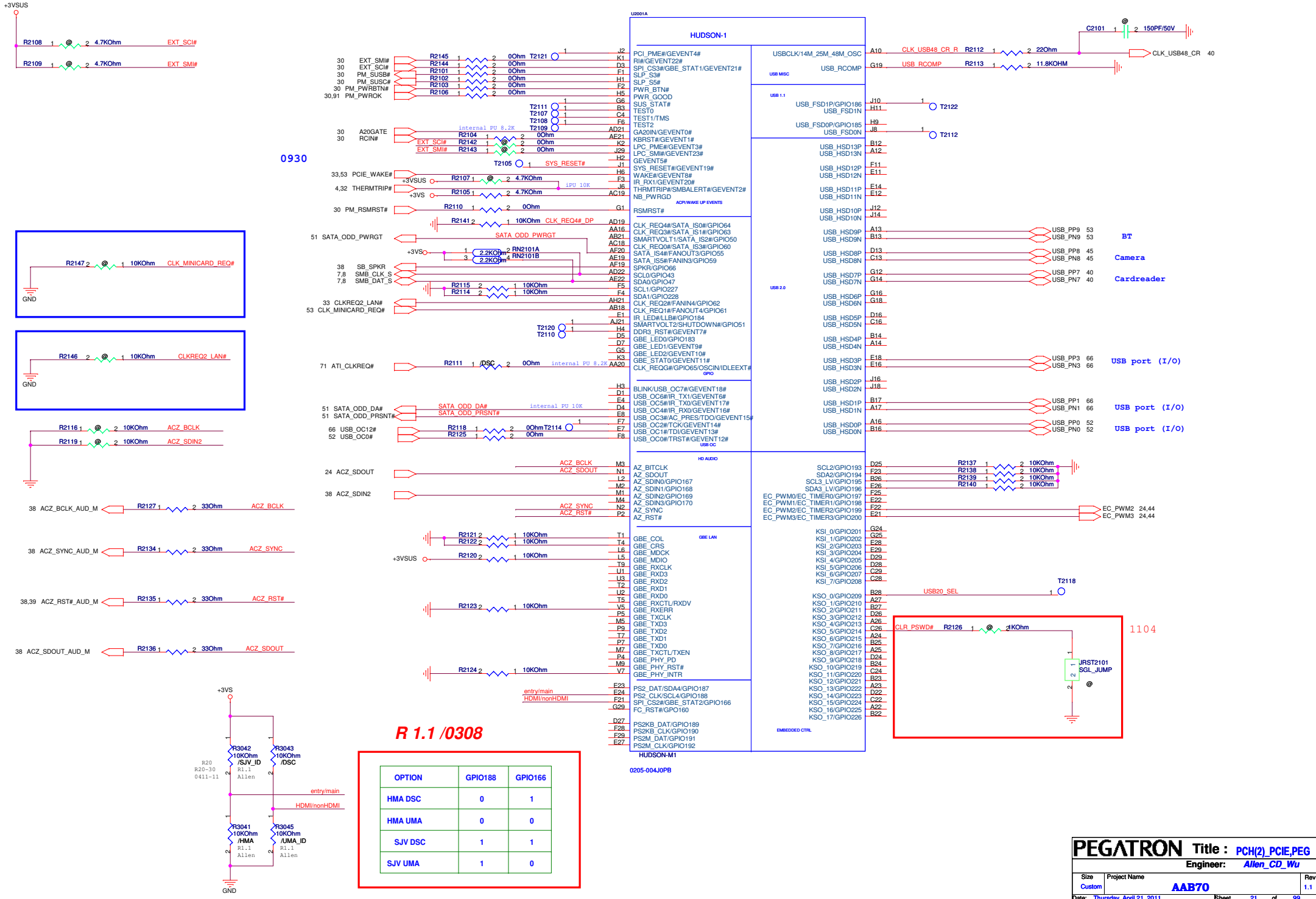
+3VSUS
A_RST#
U2002 @ SN74LVC1G08DCKR
R2018 33Ohm PCIE_ARST# 45
R2001 33Ohm BUF_PLT_RST# 30,32
C2022 150PF/50V
C2023 150PF/50V
SP2002 NB_R0402_20MIL_SMALL
1213

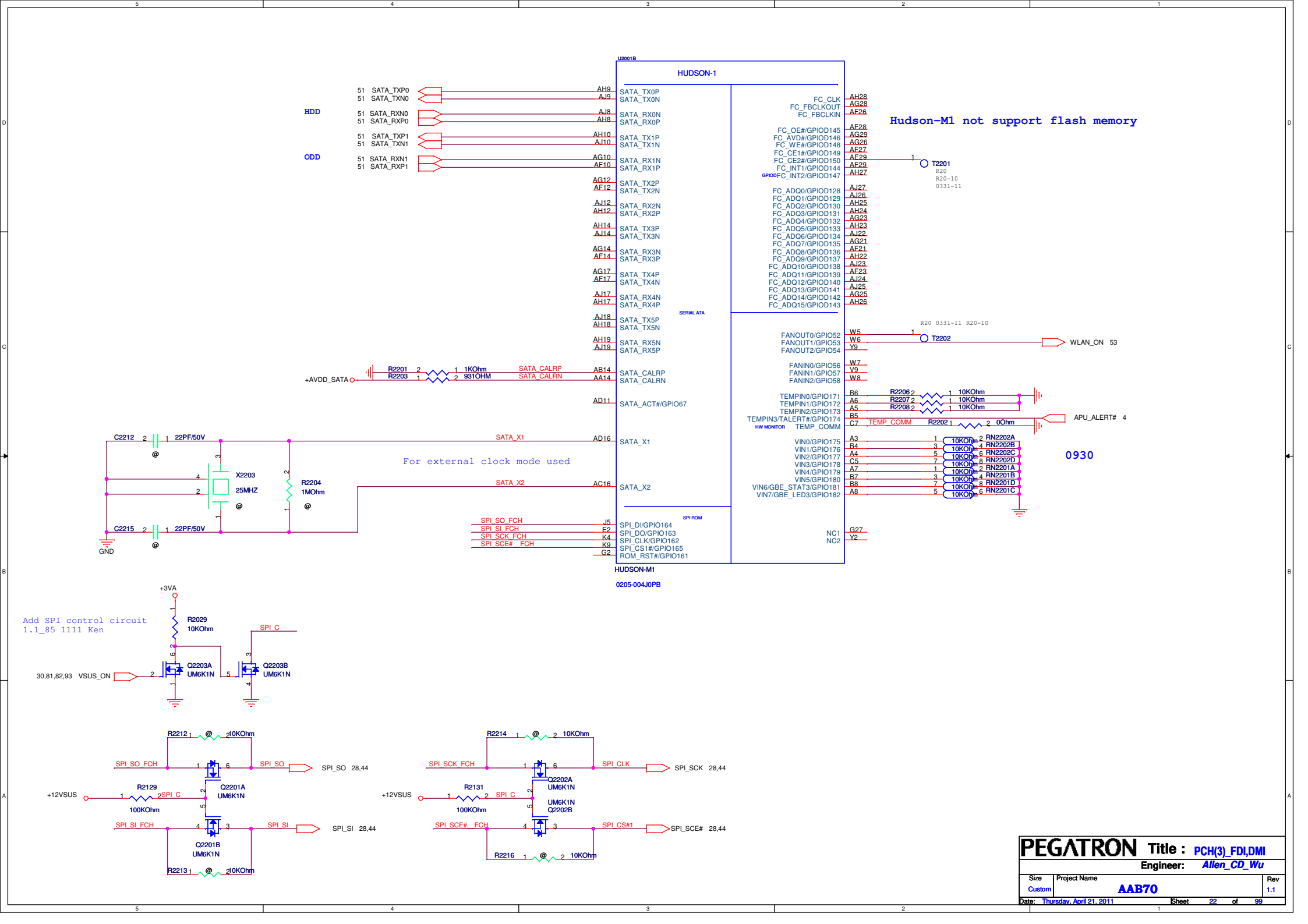
PCIERST#
U2003 @ SN74LVC1G08DCKR
R2004 33Ohm PCIE_RST# 33,53
C2021 150PF/50V
SP2003 NB_R0402_20MIL_SMALL
1213

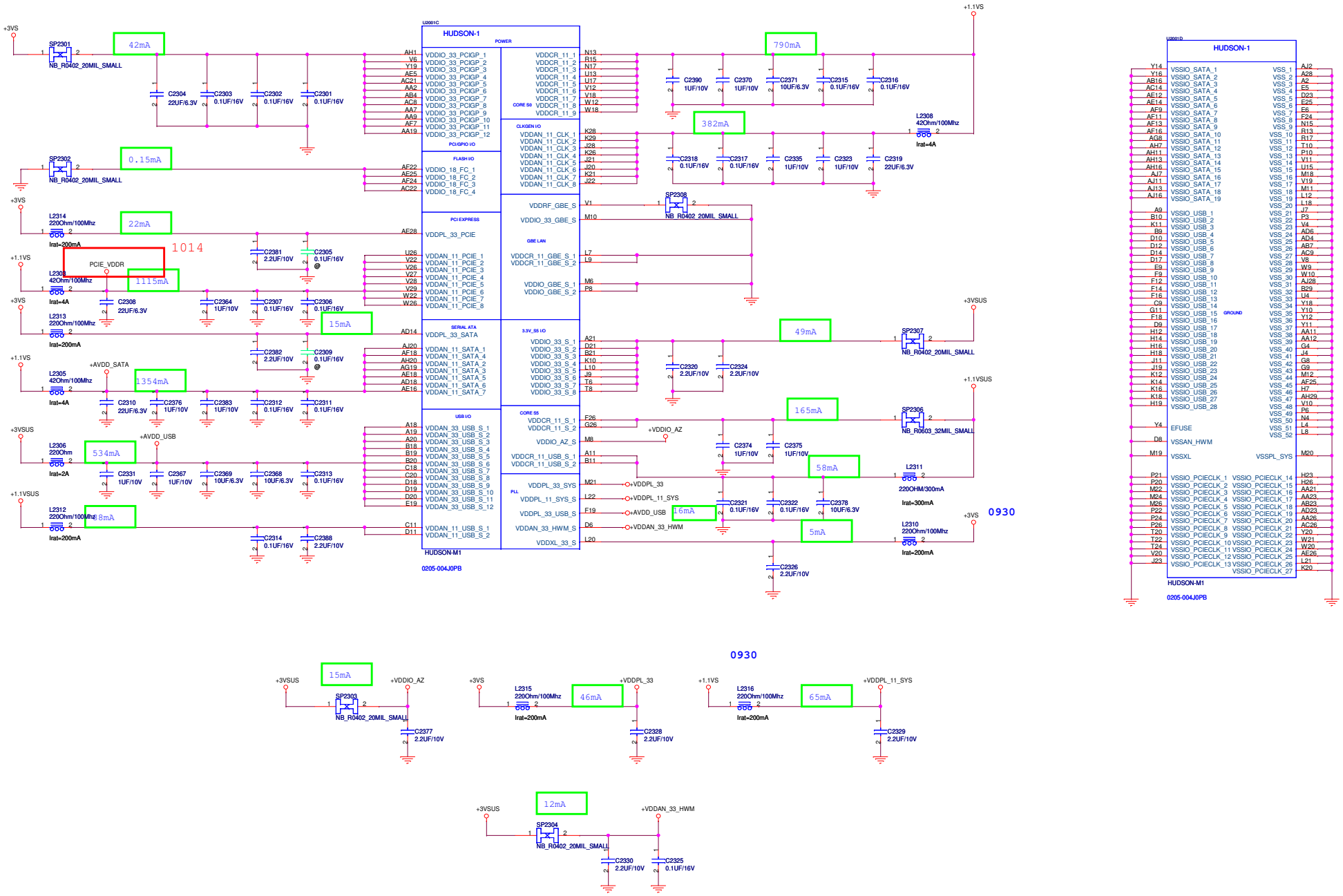
PCIE_RST# is for PCIE device in Hudson

CLK_KBCPCI C2024 150PF/50V @
+3VSUS
PE_GPIO0
PCIE_ARST#
U2005 SN74LVC1G08DCKR
dGPU_RST# 70
R2009 0Ohm @

check 0125

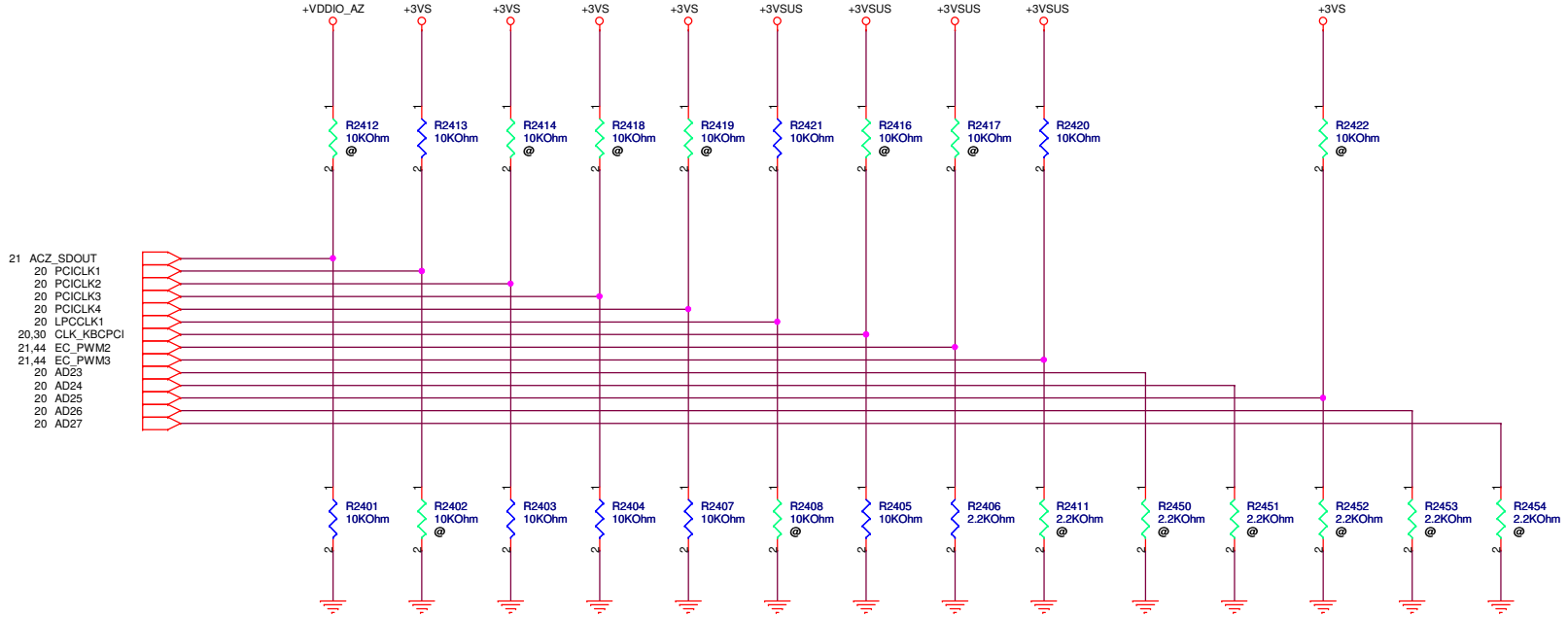

HUDSON-1
HUDSON-M1
0205-004J0PB
0930
R 1.1 /0308
1104
PEGATRON
Title : PCH(2)_PCIE,PEG
Engineer: Allen_CD_Wu
Size Custom
Project Name AAB70
Rev 1.1
Date: Thursday, April 21, 2011
Sheet 21 of 99
BT
Camera
Cardreader
USB port (I/O)
USB port (I/O)
USB port (I/O)
OPTION | GPIO188 | GPIO166
HMA DSC | 0 | 1
HMA UMA | 0 | 0
SJV DSC | 1 | 1
SJV UMA | 1 | 0


U2001B
HUDSON-1
HDD
ODD
SERIAL ATA
SPI ROM
HUDSON-M1
0205-004J0PB
Hudson-M1 not support flash memory
T2201
T2202
WLAN_ON 53
APU_ALERT# 4
For external clock mode used
0930
Add SPI control circuit
1.1_85 1111 Ken
+3VA
VSUS_ON
+12VSUS
GND
+AVDD_SATA
SPI_SO 28,44
SPI_SCK 28,44
SPI_SI 28,44
SPI_SCE# 28,44
PEGATRON
Title : PCH(3)_FDI,DMI
Engineer: Allen_CD_Wu
Size Custom
Project Name AAB70
Rev 1.1
Date: Thursday, April 21, 2011
Sheet 22 of 99



PEGATRON	Title : PCH(4)_DP,LVDS,CRT		
	Engineer: Allen_CD_Wu		
Size: C	Project Name: AAB70		Rev: 1.1
Date: Monday, March 21, 2011	Sheet 23 of 99		

Strap Pins



	ACZ_SDOUT_AUD	PCICLK1	PCICLK2	PCICLK3	PCICLK4	LPCCLK0 CLK_KBCPCI	LPCCLK1	EC_PWM2	EC_PWM3	
High	low power mode	***PCIE Gen2***	watchdog timer enable	debug	no-Fusion clock mode	EC enable	***clock gen. enable***	H	L	LPC ROM
Low	***peformance mode***	PCIE Gen1	***watchdog timer disable***	***ignore debug***	***Fusion clock mode***	***EC disable***	clock gen. disable	L	H	SPI ROM

Debug Straps

	AD23	AD24	AD25	AD26	AD27
High	***disable PCI mem boot***	***default PCIE straps***	***use FC PLL***	***disable ILA autorun***	***use PCI PLL***
Low	enable PCI mem boot	EEPROM PCIE straps	bypass FC PLL	enable ILA autorun	by pass PCI PLL

PEGATRON Title : PCH(5)_PCI,USB

Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

Date: Thursday, April 21, 2011 Sheet 24 of 99

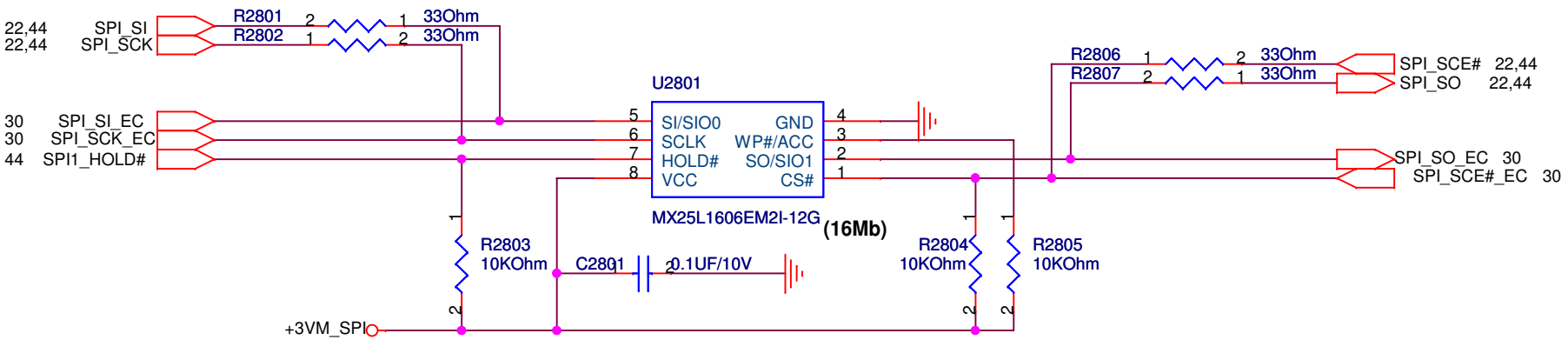
PEGATRON

Title : PCH(6)_CPU,GPIO,MISC

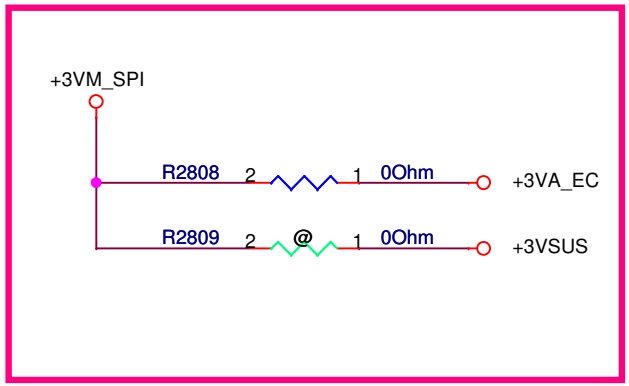
Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

Date: Monday, March 21, 2011 Sheet 25 of 99



1110



WINBOND:0500-00P4000
MXIC: 0500-00TY000

reserved for BIOS testing

PEGATRON	Title : SPI ROM	
	Engineer: Allen_CD_Wu	
Size: A	Project Name: BS_AB	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 28 of 99	

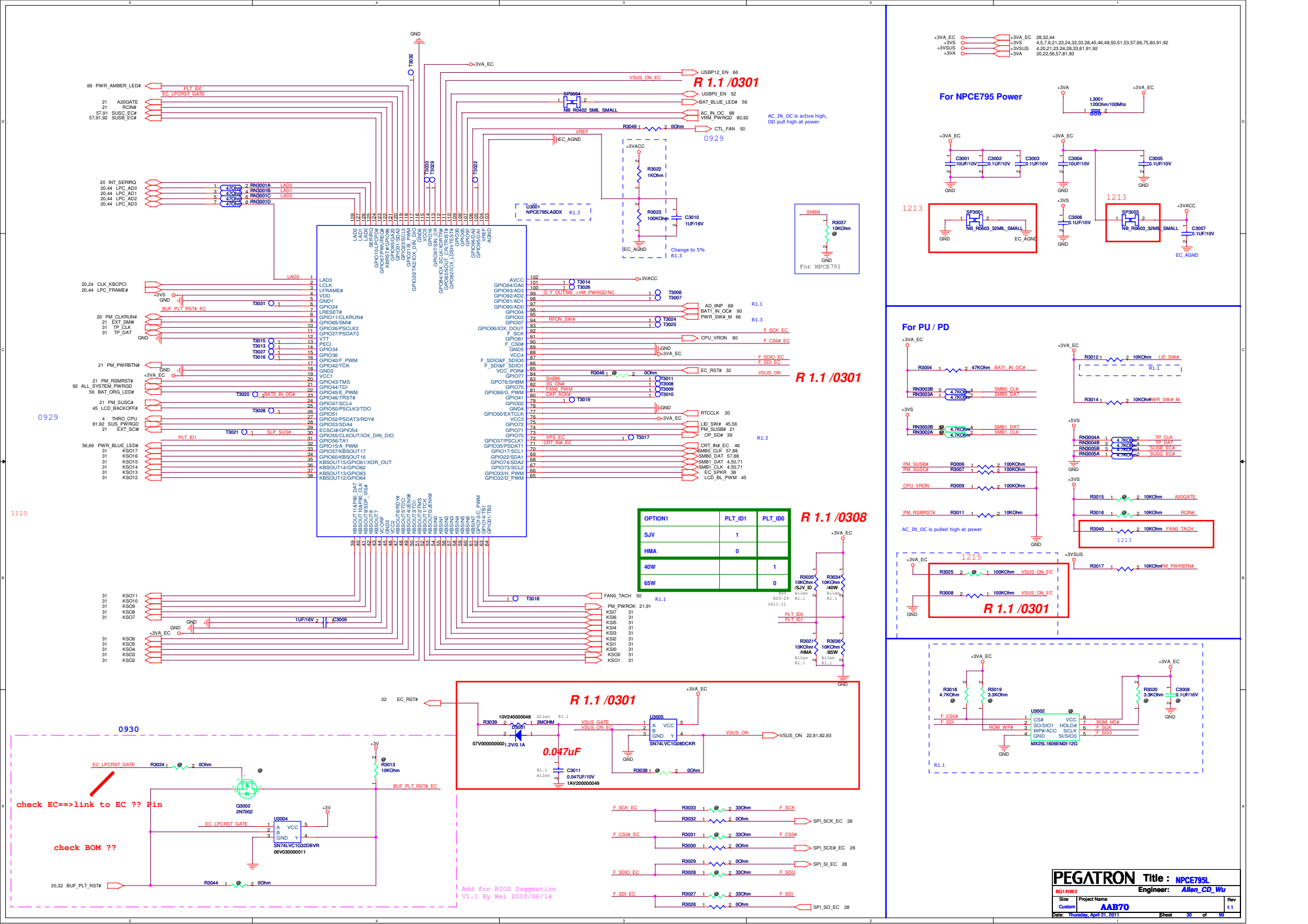
PEGATRON

Title : CLK_SLG8SP585VTR

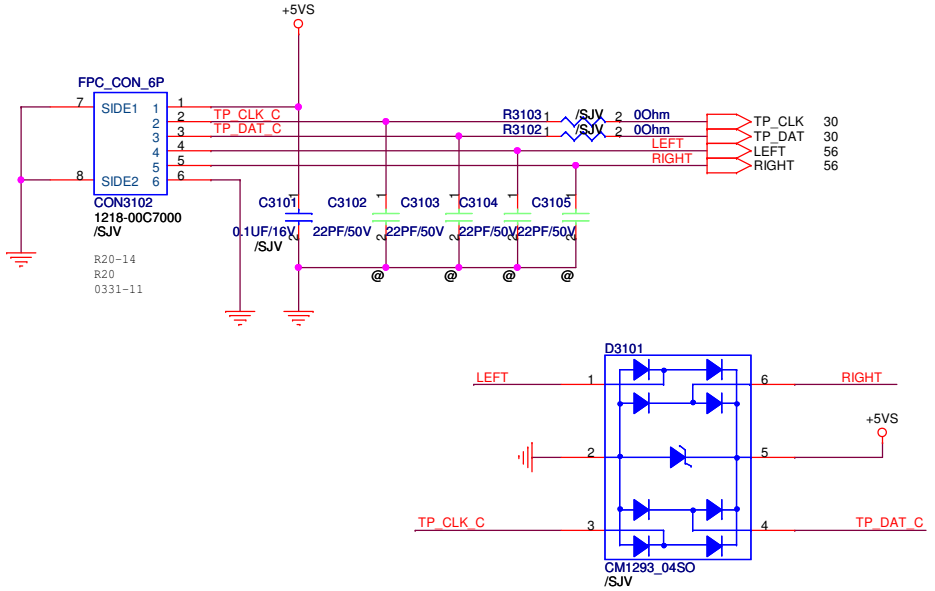
Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

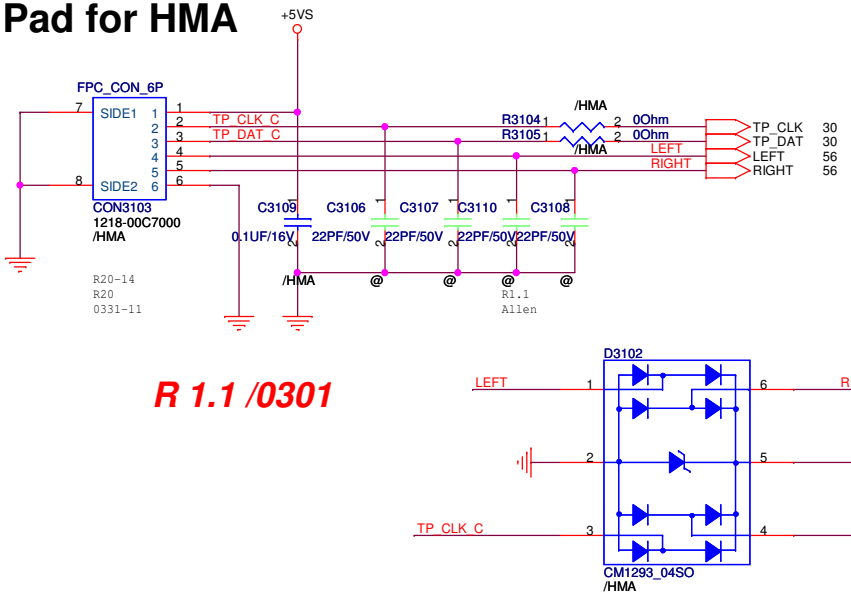
Date: Monday, March 21, 2011 Sheet 29 of 99


For NPCE795 Power
For PU / PD
R 1.1 /0301
R 1.1 /0308
0929
0930
1110
1213
1215
check EC==>link to EC ?? Pin
check BOM ??
Add for BIOS Suggestion
V1.1 By Wei 2010/06/14
AC_IN_OC is active high, OD pull high at power
AC_IN_OC is pulled high at power
Change to 5%
For NPCE791
OPTION1 | PLT_ID1 | PLT_ID0
SJV | 1 |
HMA | 0 |
40W | | 1
65W | | 0
PEGATRON
Title : NPCE795L
BG1/HW2
Engineer: Allen_CD_Wu
Size: Custom
Project Name: AAB70
Rev: 1.1
Date: Thursday, April 21, 2011
Sheet 30 of 99

Touch Pad for SJV



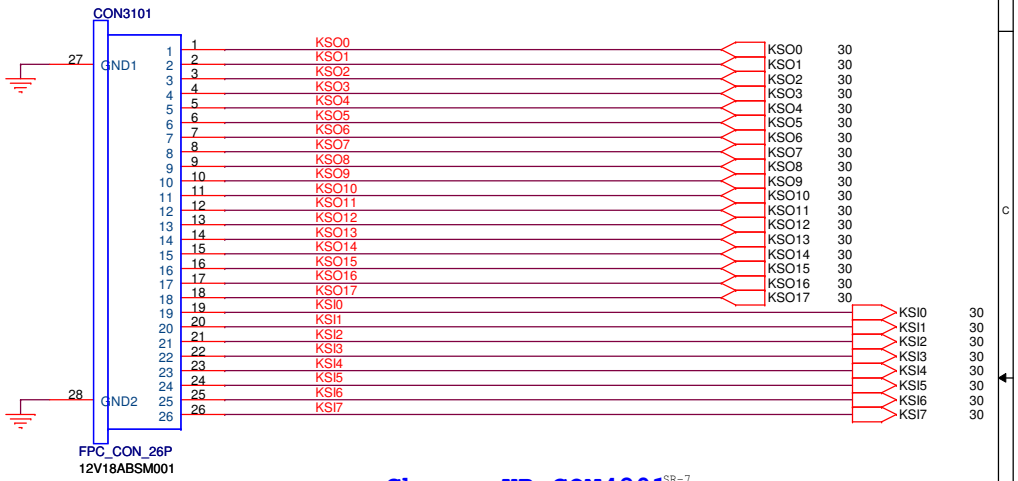
Touch Pad for HMA



R 1.1 /0301

Keyboard FOR 17"

AAB70 0124



Change KB CON4801 SR-7 0118-11

PEGATRON **Title :** EC_IT8512(2)KB, TP FP

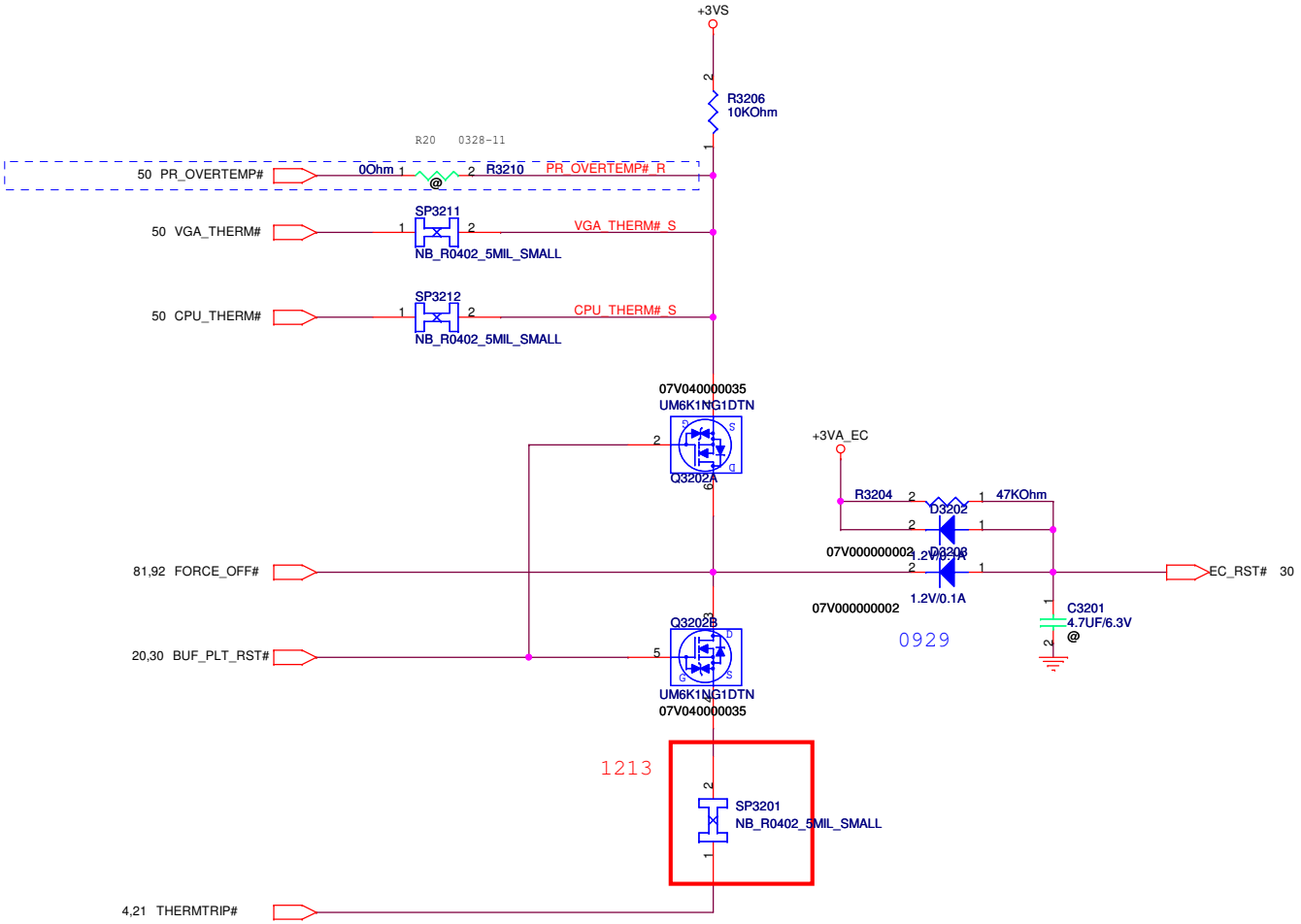
BG1/HW2 **Engineer:** *Allen_CD_Wu*

Size	Project Name	Rev
B	**AAB70**	1.1

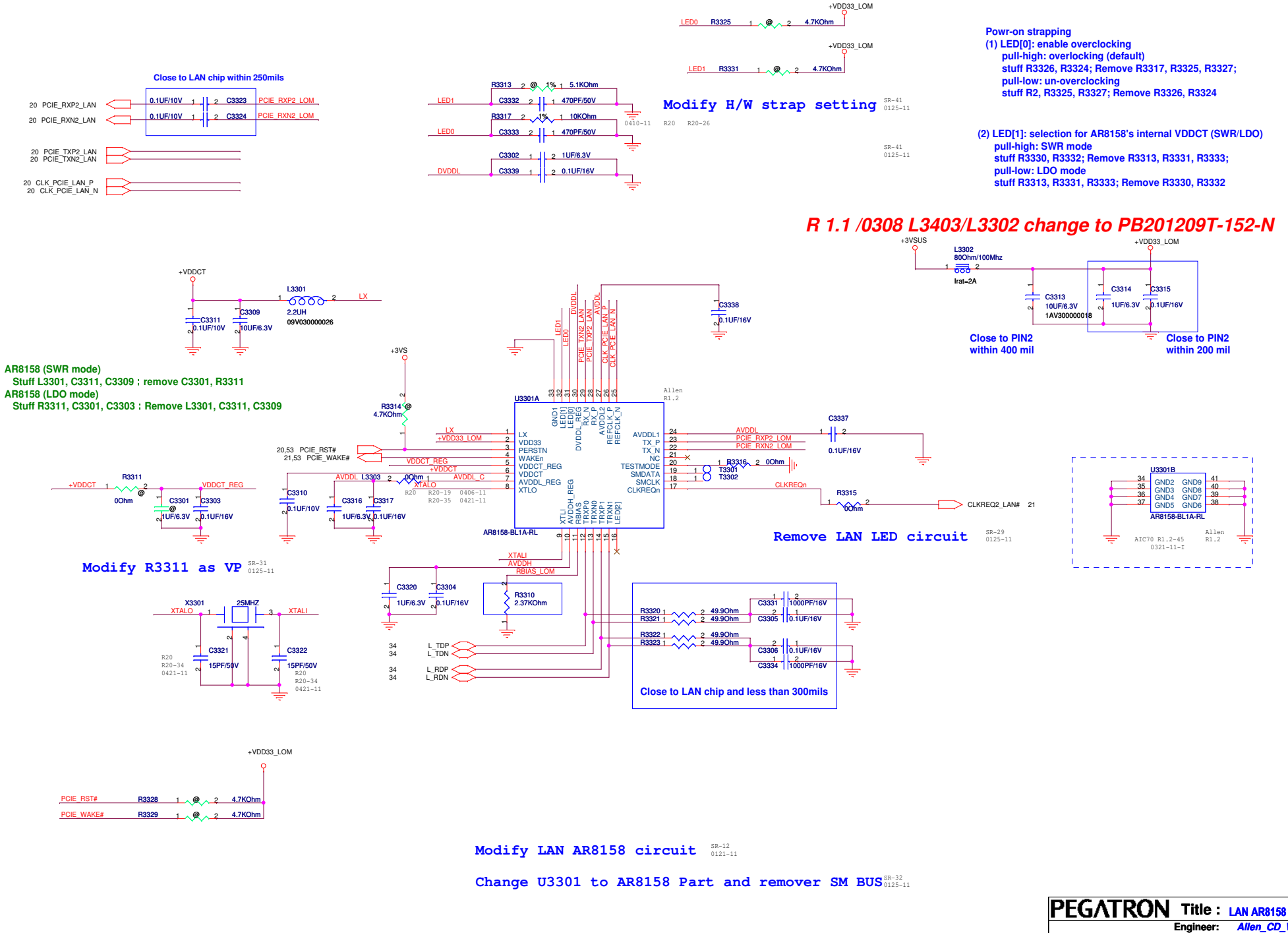
Date: Thursday, April 21, 2011 Sheet 31 of 99

Thermal Policy

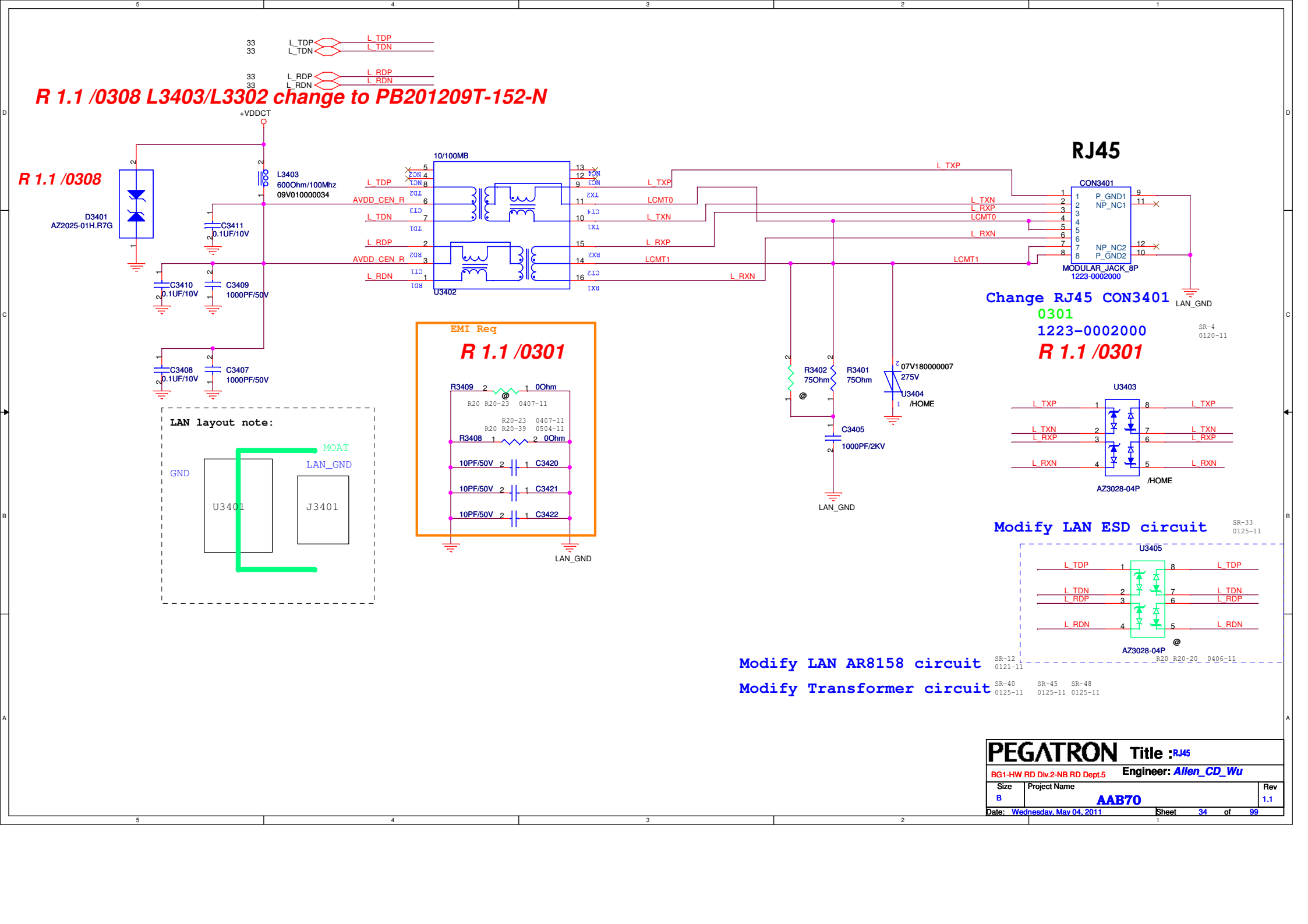
NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us



PEGATRON	Title : RST_Reset Circuit	
	Engineer: Allen_CD_Wu	
Size: B	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 32 of 99	



PEGATRON	Title : LAN AR8158		
	Engineer: Allen_CD_Wu		
Size: Custom	Project Name: BS_AB		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 33 of 99		

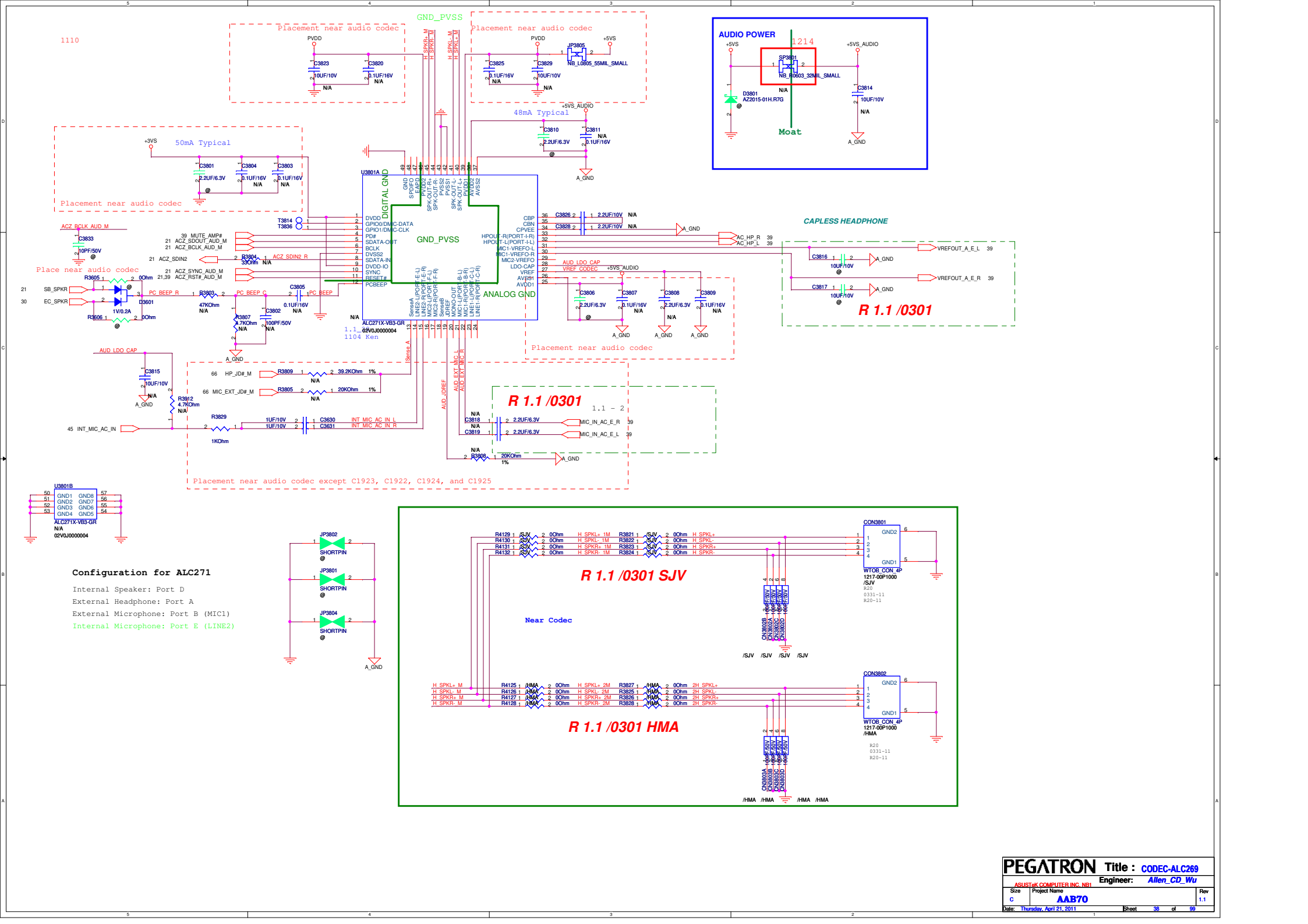

R 1.1 /0308 L3403/L3302 change to PB201209T-152-N
33 L_TDP
33 L_TDN
L_TDP
L_TDN
33 L_RDP
33 L_RDN
L_RDP
L_RDN
+VDDCT
R 1.1 /0308
D3401
AZ2025-01H.R7G
L3403
600Ohm/100Mhz
09V010000034
C3411
0.1UF/10V
C3410
0.1UF/10V
C3409
1000PF/50V
C3408
0.1UF/10V
C3407
1000PF/50V
10/100MB
U3402
AVDD_CEN_R
L_TXP
L_TXN
L_RXP
L_RXN
LCMT0
LCMT1
RJ45
CON3401
P_GND1
NP_NC1
NP_NC2
P_GND2
MODULAR_JACK_8P
1223-0002000
LAN_GND
Change RJ45 CON3401
0301
1223-0002000
R 1.1 /0301
SR-4
0120-11
EMI Req
R 1.1 /0301
R3409 0Ohm
R20 R20-23 0407-11
R20-23 0407-11
R20 R20-39 0504-11
R3408 0Ohm
10PF/50V C3420
10PF/50V C3421
10PF/50V C3422
LAN_GND
R3402 75Ohm
R3401 75Ohm
07V180000007
275V
U3404
/HOME
C3405
1000PF/2KV
LAN_GND
U3403
AZ3028-04P
/HOME
LAN layout note:
MOAT
LAN_GND
GND
U3401
J3401
Modify LAN ESD circuit
SR-33
0125-11
U3405
AZ3028-04P
R20 R20-20 0406-11
Modify LAN AR8158 circuit
SR-12
0121-11
Modify Transformer circuit
SR-40
0125-11
SR-45
0125-11
SR-48
0125-11
PEGATRON
Title :RJ45
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Allen_CD_Wu
Size
B
Project Name
AAB70
Rev
1.1
Date: Wednesday, May 04, 2011
Sheet 34 of 99

PEGATRON Title : MDC CONN

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Allen_CD_Wu

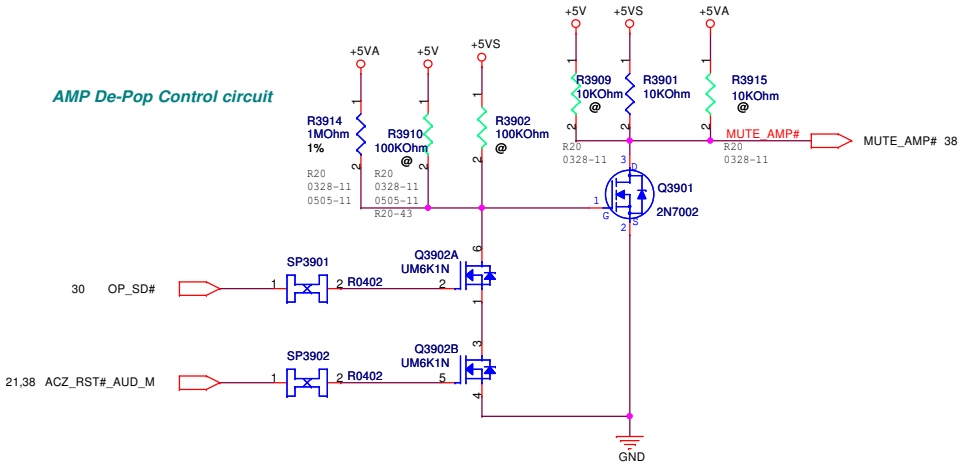
Size	Project Name	Rev
C	AAB70	1.1

Date: Monday, March 21, 2011 Sheet 35 of 99



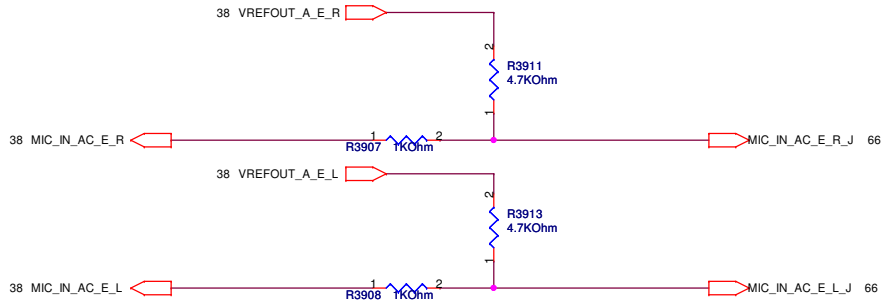
PEGATRON	Title : CODEC-ALC269	
	Engineer: Allen_CD_Wu	
ASUSTeK COMPUTER INC. NB1		
Size: C	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 38 of 99	

AMP De-Pop Control circuit



R 1.1 /0301

1.1 - 2
1.1 - 22

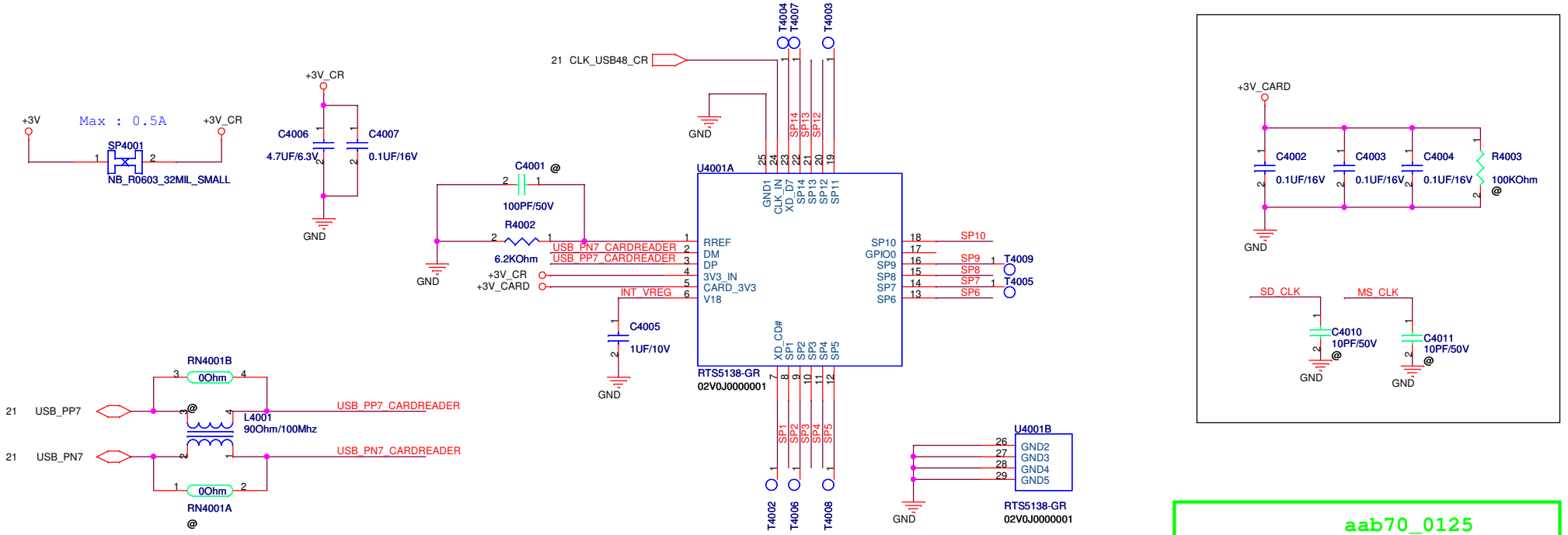


PEGATRON Title : AUDIO ALC269

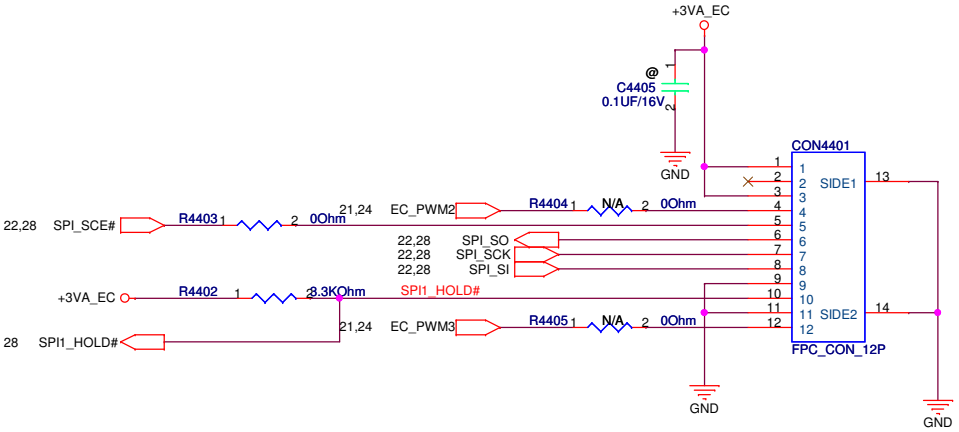
BU1-RD Div.1-HW RD Dept.1 Engineer: Allen_CD_Wu

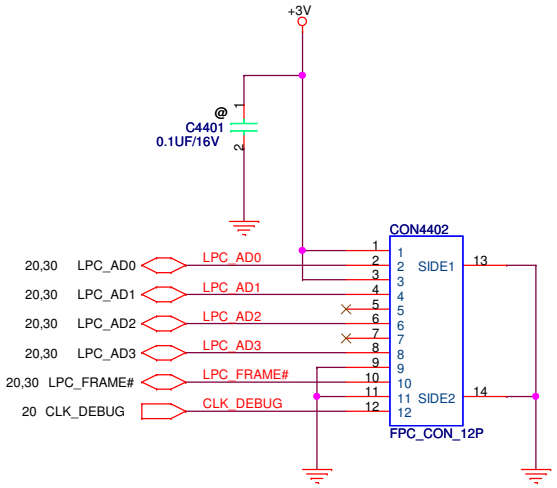
Size	Project Name	Rev
Custom	AAB70	1.1

Date: Thursday, May 05, 2011 Sheet 39 of 99



PEGATRON	Title : RTS 5138	
PEGATRON CORPORATION	Engineer:	
Size: B	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 40 of 99	



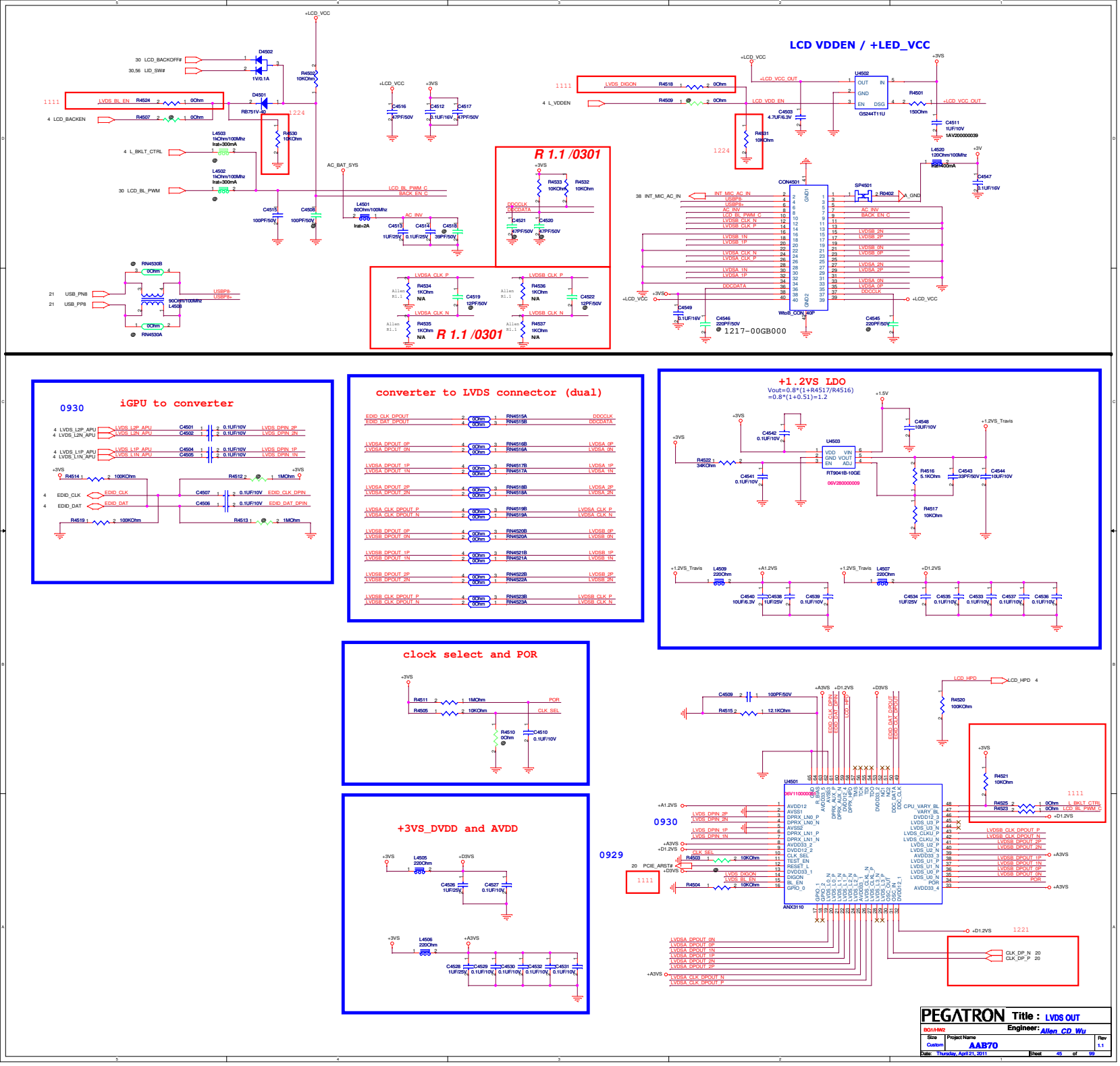


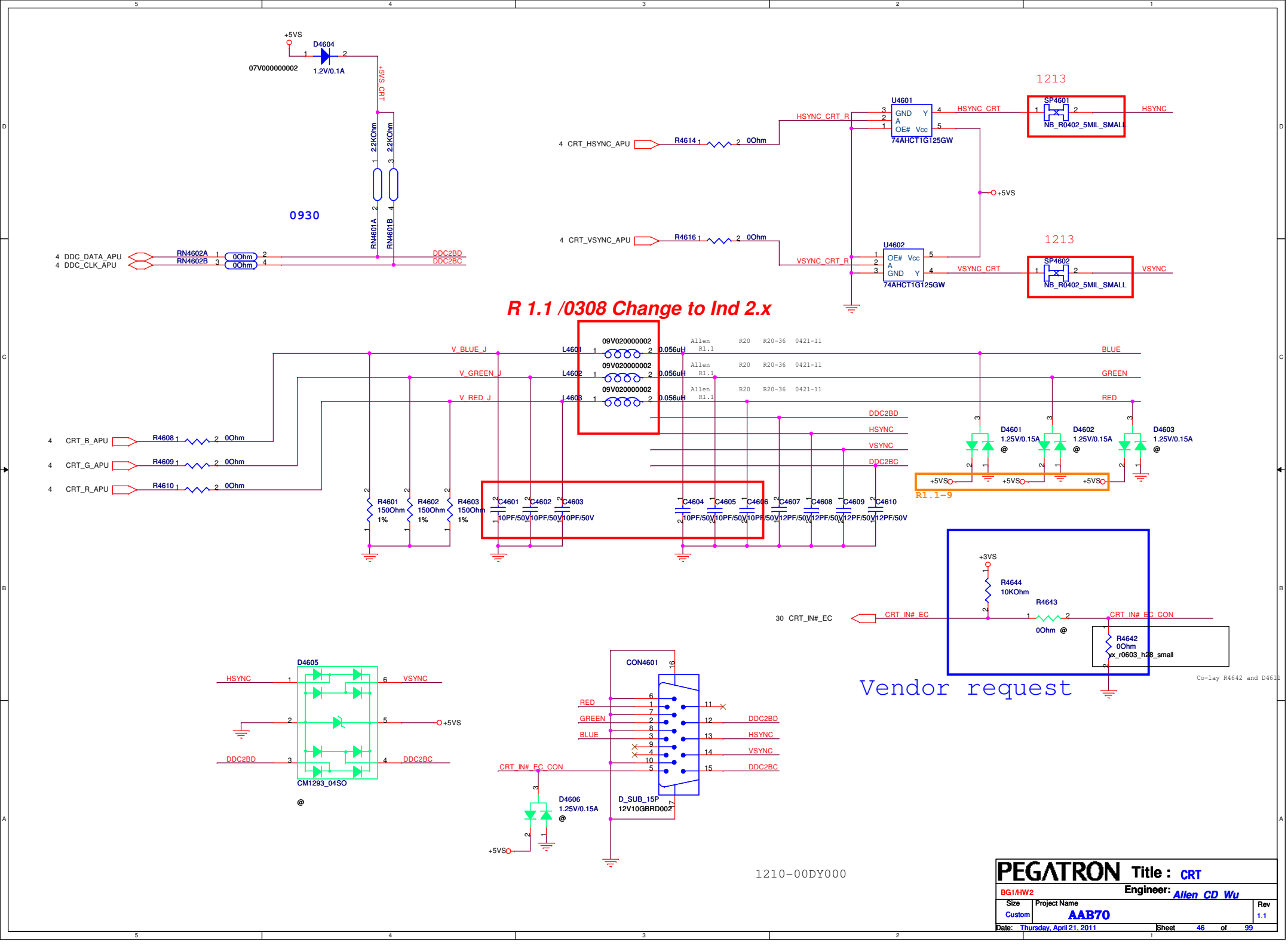
PEGATRON **Title : DEBUG**

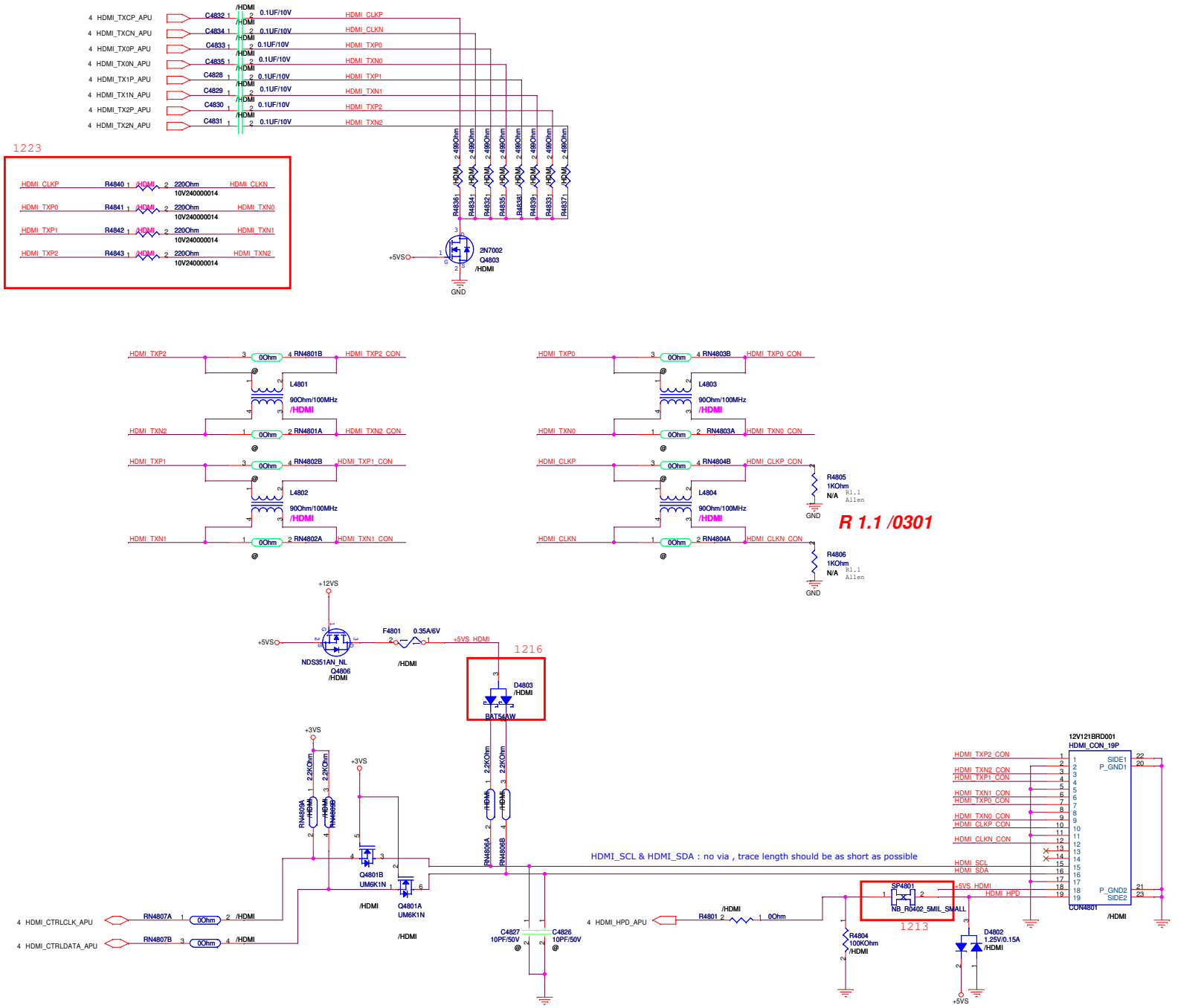
BG1/HW2 **Engineer: *Allen CD Wu***

Size	Project Name	Rev
B	**AAB70**	1.1

Date: Thursday, April 21, 2011 Sheet 44 of 99

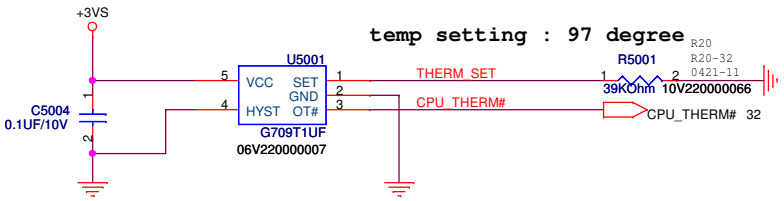

LCD VDDEN / +LED_VCC
R 1.1 /0301
R 1.1 /0301
iGPU to converter
0930
converter to LVDS connector (dual)
+1.2VS LDO
Vout=0.8*(1+R4517/R4516)
=0.8*(1+0.51)=1.2
clock select and POR
+3VS_DVDD and AVDD
0930
0929
1217-00GB000
PEGATRON
Title : LVDS OUT
Engineer: Allen_CD_Wu
Project Name
AAB70
Rev
1.1
Thursday, April 21, 2011
Sheet 45 of 99


+5VS
D4604
07V000000002
1.2V/0.1A
+5VS_CRT
2.2KOhm
2.2KOhm
RN4601A
RN4601B
0930
4 DDC_DATA_APU
4 DDC_CLK_APU
RN4602A
RN4602B
0Ohm
0Ohm
DDC2BD
DDC2BC
1213
U4601
GND Y
A
OE# Vcc
74AHCT1G125GW
HSYNC_CRT_R
HSYNC_CRT
SP4601
NB_R0402_5MIL_SMALL
HSYNC
4 CRT_HSYNC_APU
R4614
0Ohm
+5VS
4 CRT_VSYNC_APU
R4616
0Ohm
U4602
OE# Vcc
A
GND Y
74AHCT1G125GW
VSYNC_CRT_R
VSYNC_CRT
SP4602
NB_R0402_5MIL_SMALL
VSYNC
R 1.1 /0308 Change to Ind 2.x
V_BLUE_J
V_GREEN_J
V_RED_J
L4601
L4602
L4603
09V020000002
0.056uH
Allen R20 R20-36 0421-11 R1.1
BLUE
GREEN
RED
DDC2BD
HSYNC
VSYNC
DDC2BC
4 CRT_B_APU
4 CRT_G_APU
4 CRT_R_APU
R4608
R4609
R4610
0Ohm
R4601
R4602
R4603
150Ohm
1%
C4601
C4602
C4603
C4604
C4605
C4606
C4607
C4608
C4609
C4610
10PF/50V
12PF/50V
D4601
D4602
D4603
1.25V/0.15A
@
R1.1-9
+3VS
R4644
10KOhm
R4643
0Ohm @
30 CRT_IN#_EC
CRT_IN#_EC
CRT_IN#_EC_CON
R4642
0Ohm
xx_r0603_h28_small
Co-lay R4642 and D4611
Vendor request
D4605
HSYNC
VSYNC
DDC2BD
DDC2BC
+5VS
CM1293_04SO
@
CON4601
D_SUB_15P
12V10GBRD002
D4606
1.25V/0.15A
@
1210-00DY000
PEGATRON
Title : CRT
BG1/HW2
Engineer: Allen_CD_Wu
Size
Custom
Project Name
AAB70
Rev
1.1
Date: Thursday, April 21, 2011
Sheet 46 of 99

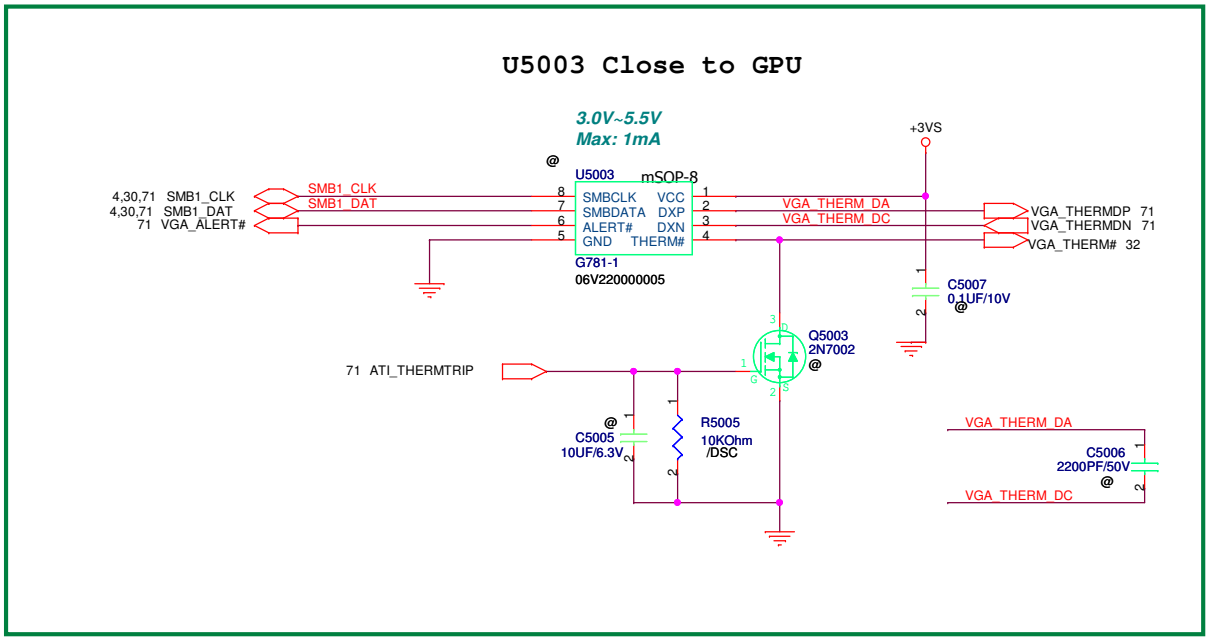


PEGATRON	Title : HDMI Connector		
BG1/HW2	Engineer: Allen_CD_Wu		
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 48 of 99		

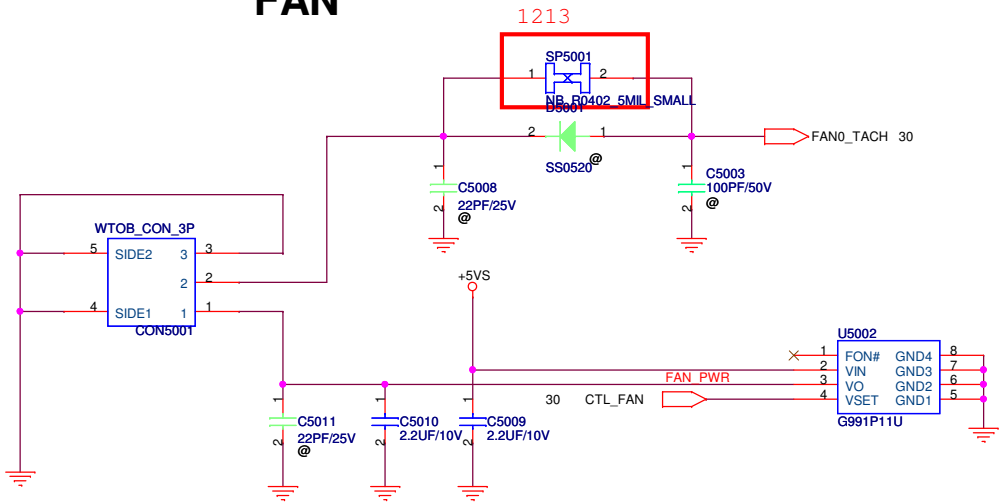
U5001 Close to CPU



U5003 Close to GPU

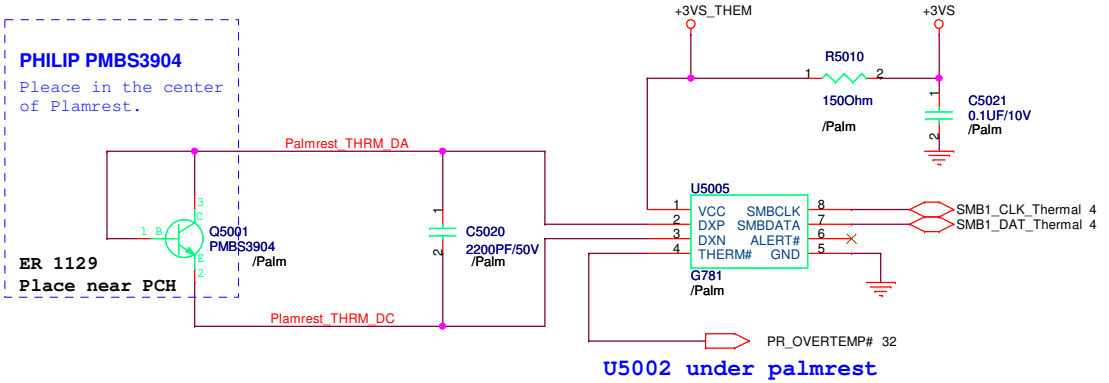


FAN



Plam Rest Thermal Sensor

R20 0328-11
R20-9 0330-11



U5002 under palmrest

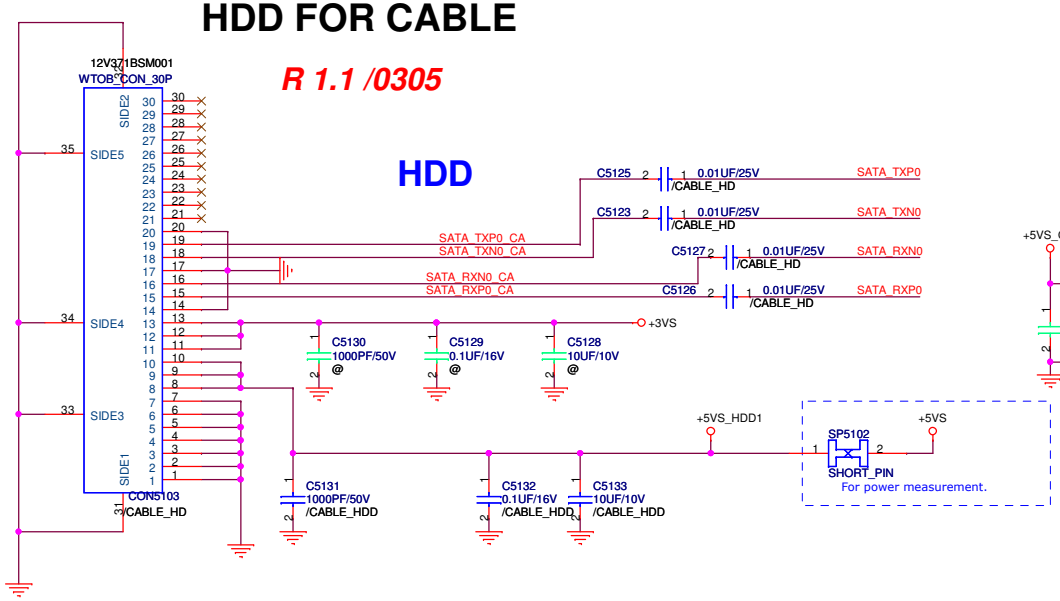
SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

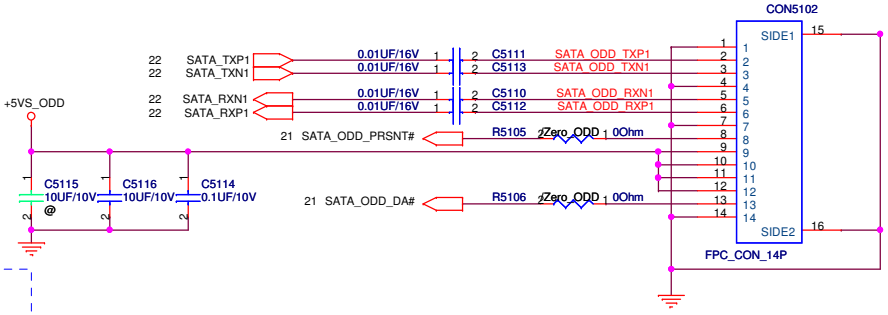
PEGATRON	Title : FAN_Fan,Sensor	
	Engineer: Allen_CD_Wu	
Size: B	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 50 of 99	

HDD FOR CABLE

R 1.1 /0305

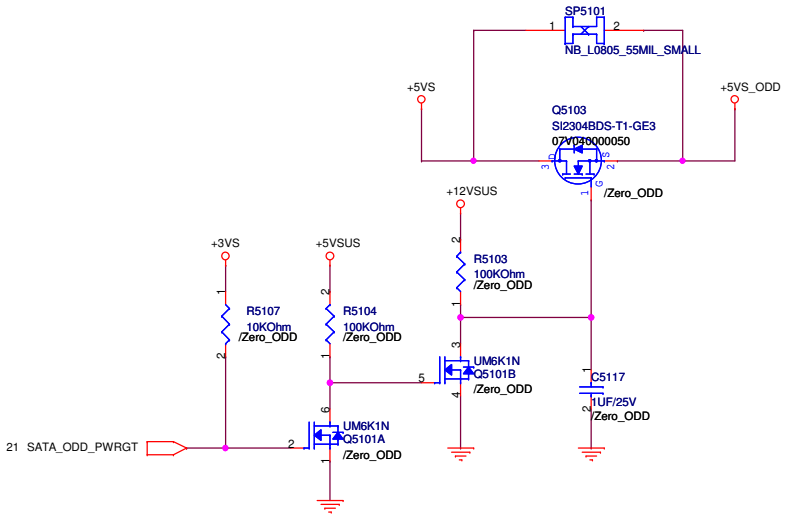


ODD FOR 17"

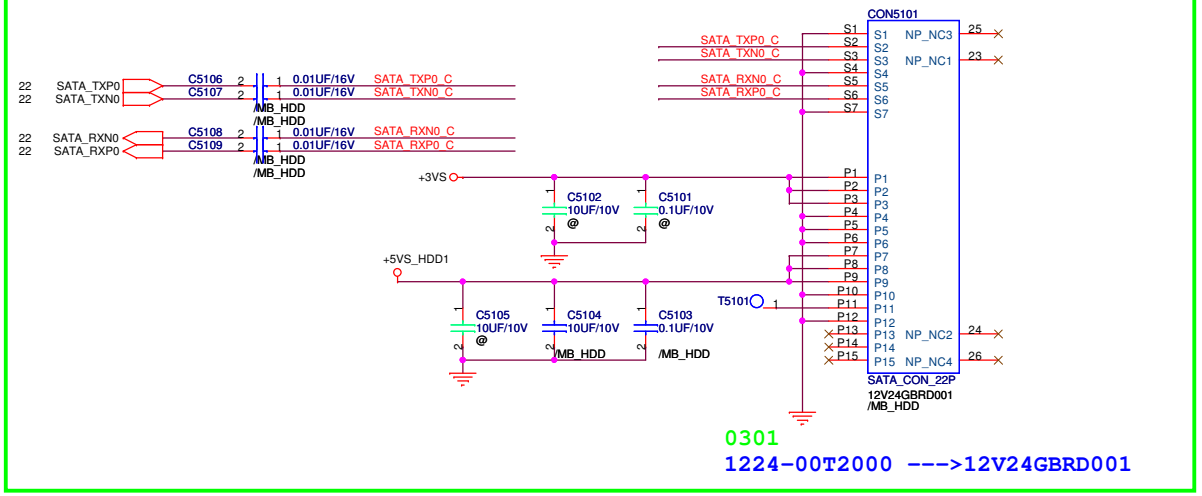


ZERO POWER ODD SUPPORT

support Hokey turn off ODD power

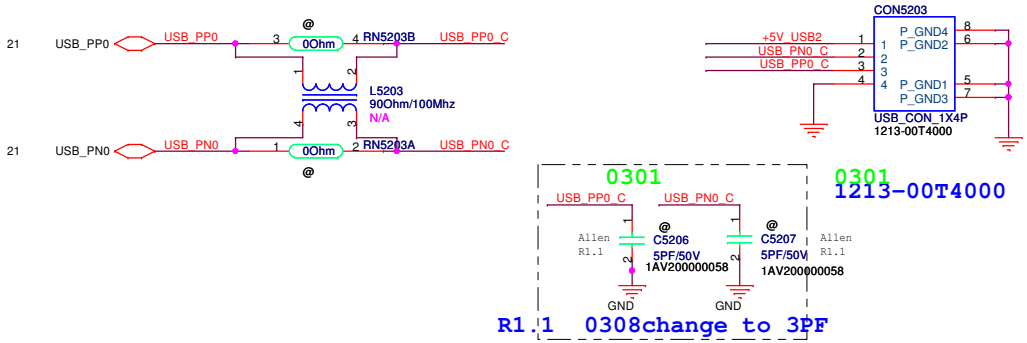


HDD 0129



PEGATRON	Title : HDD & CD-ROM	
BG1/HW2	Engineer: Allen_CD_Wu	
Size: Custom	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 51 of 99	

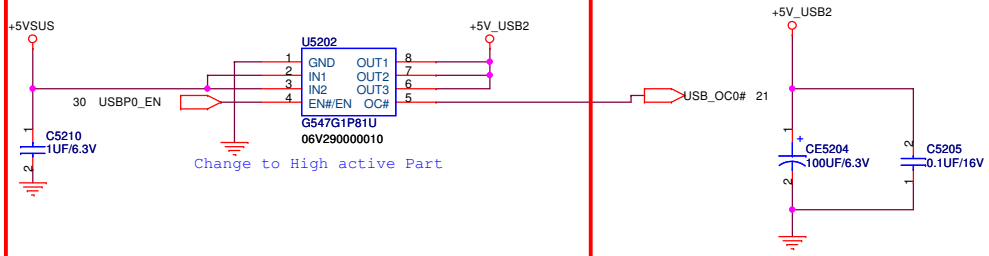
USB 2.0



0301
1213-00T4000

R1.1 0308change to 3PF

AAB70



PEGATRON Title : USB PORTS/ eSATA

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

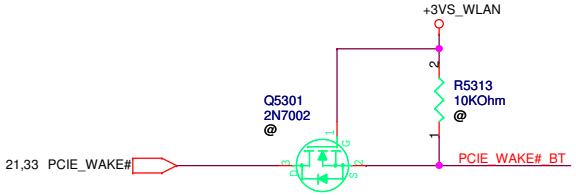
Date: Thursday, April 21, 2011 Sheet 52 of 99

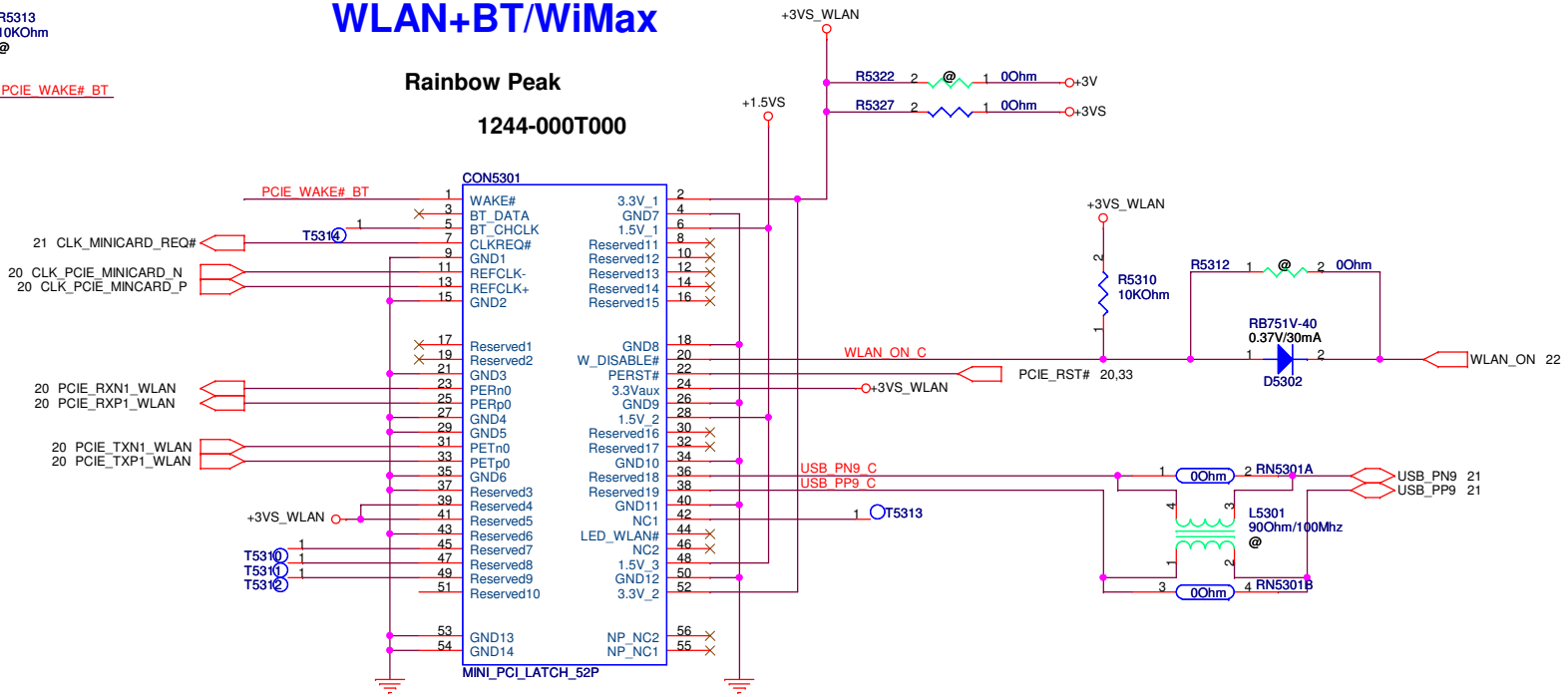
1001

WLAN+BT/WiMax

Rainbow Peak

1244-000T000



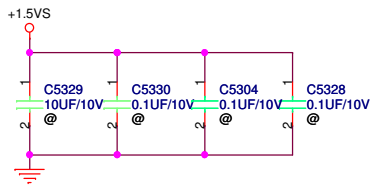


H = 6.5 mm

WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

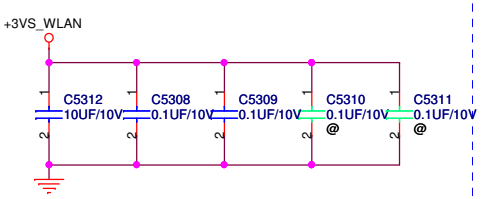
Place 10UF near +1.5VS source side.



WLAN +3VS bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VS_WLAN source side.



PEGATRON	Title : MINICARD Wireless	
BG1/HW2	Engineer: Allen_CD_Wu	
Size: B	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 53 of 99	

PEGATRON Title : Mini Card HSDPA

BG1/HW2 Engineer: Allen_CD_Wu

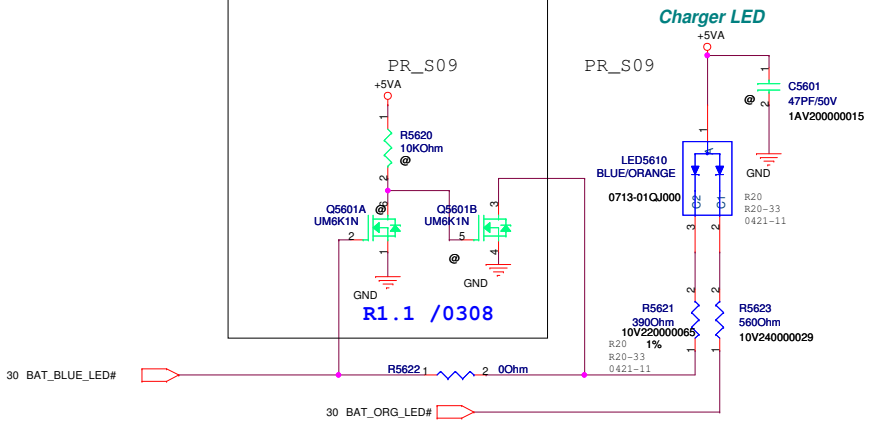
Size	Project Name	Rev
Custom	AAB70	1.1

Date: Monday, March 21, 2011 Sheet 54 of 99

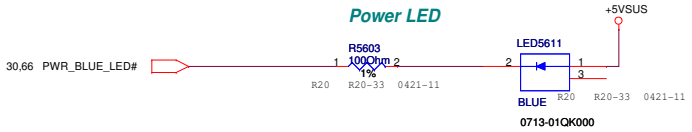
Order of Indicator LEDs

DC-IN Power Battery HDD/ODD Media WiFi

ER 1129
Combine the MOSFET

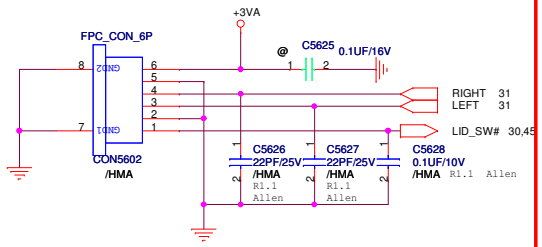


Dual Color

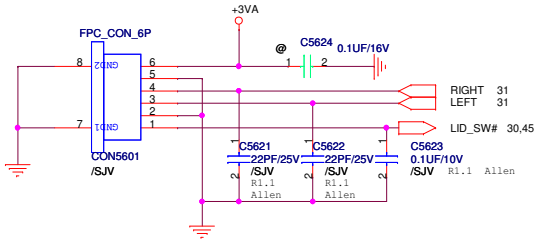


1.1

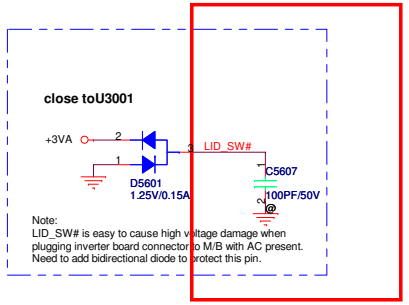
R 1.1 /0301 For HMA



For SJV

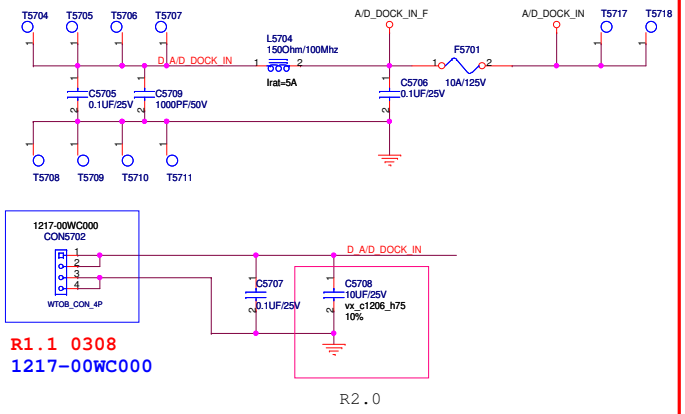


1028

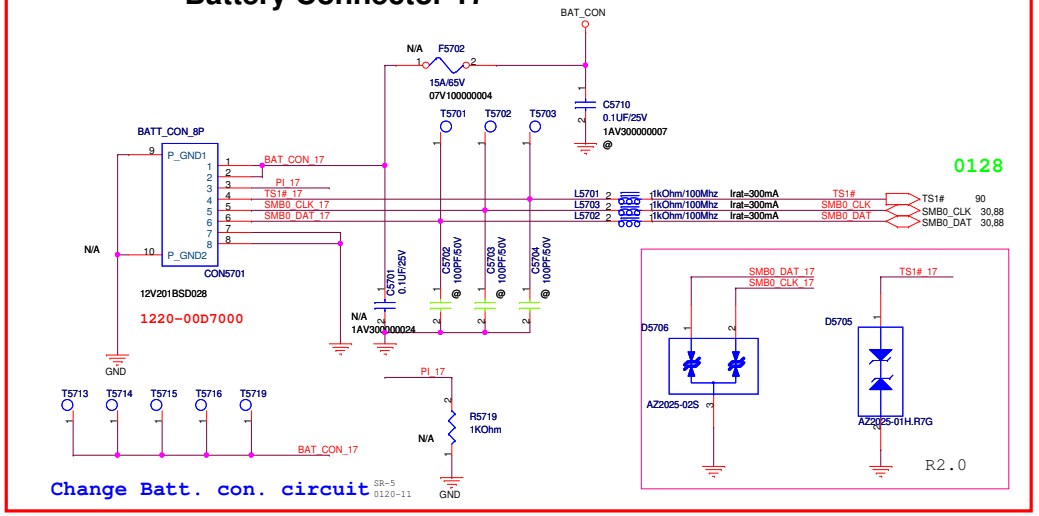


PEGATRON	Title : LED/ CIR/ FN/ SCREW	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Allen_CD_Wu	
Size: Custom	Project Name: AAB70	Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 56 of 99	

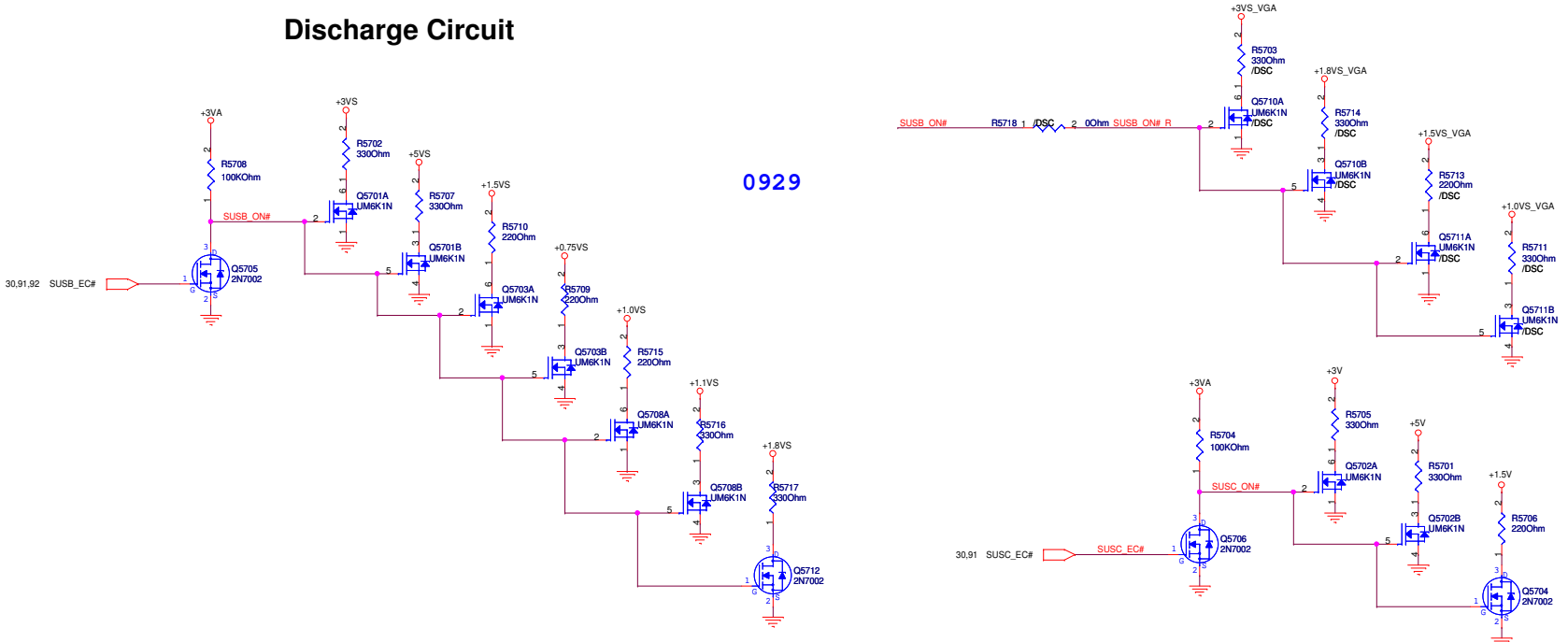
DC IN



Battery Connector 17"



Discharge Circuit



PEGATRON	Title : DISCHARGE CKT		
BG1/HW2	Engineer: Allen_CD_Wu		
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 57 of 99		

WLAN NUT

H6534

CT217B176D146

Screw Ax4
CPU

H6507
1
CRT315x335D142

H6508
1
CRT315x335D142

H6509
1
CRT315x335D142

Screw Zx1
CPU

H6634
1
CRT346X350D173

Screw Bx2
VGA

H6635
1
CRT331X346D142

H6636
1
CRT331X346D142

Local Side Symbol

FCH

H6535
@
CT236B67ID47

R20 R20-40 0504-11

H6536
@
CT236B67ID47

D

H6550
1
DO114X102N

E

H6549
1
C102D102N

Screw Cx2

H6632
1
R343x354D118

AIC70 R1.1-29 0307-11-I

SR-82

H6633
1 2 3 5 4
R354X343D118N

R20 R20-15 0404-11

Screw Ax10

H6543
1
CRT354X413CB354D118

H6540
1
C354D118

H6537
1
C354D118

H6544
1
C354D118

H6546
1
C354D118

SR-80

H6539
1 2 3 5 4
C354D118N

H6542
1 2 3 5 4
C354D118N

H6541
1 2 3 5 4
C354D118N

H6545
1 2 3 5 4
C354D118N

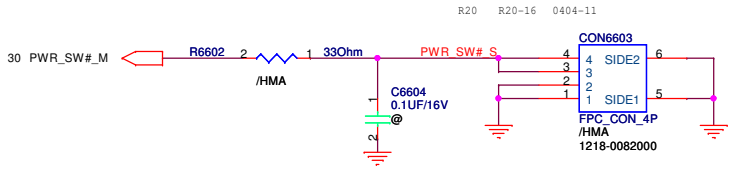
R20 R20-15 0404-11 0406-11 R20-18

PEGATRON Title : ME_CONN,Skew Hole

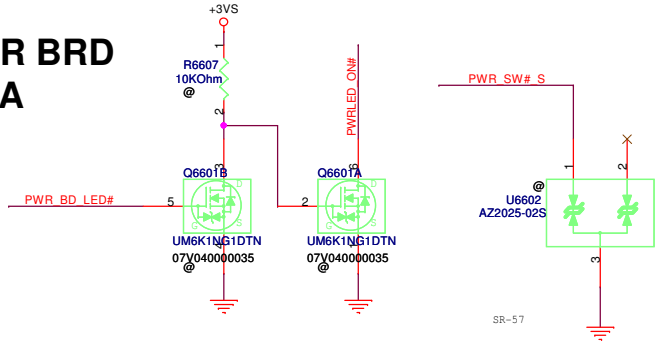
Engineer: Allen_CD_Wu

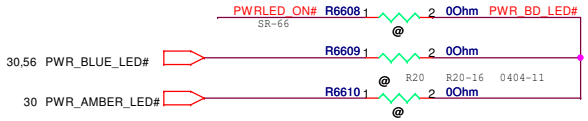
Size	Project Name	Rev
B	AAB70	1.1

Date: Wednesday, May 04, 2011 Sheet 65 of 99



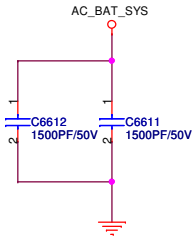
PWR BRD HMA





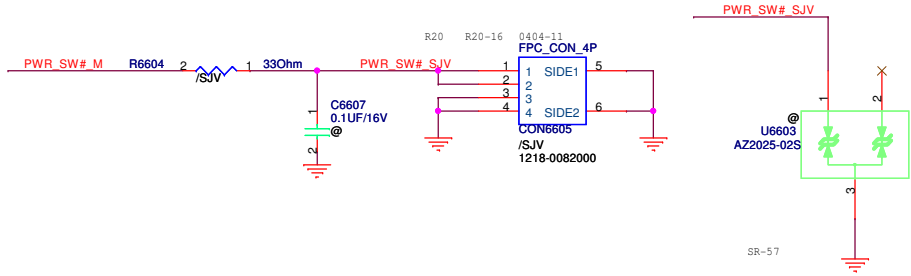
change PWR LED CON6603 circuit 0129

EMI



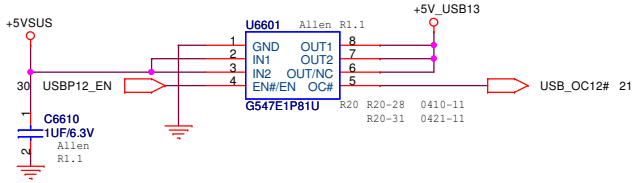
ADAPTOR VOLTAGE DETECTOR.

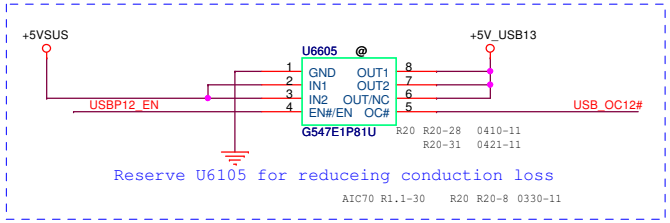
PWR SJV R 1.1 /0301

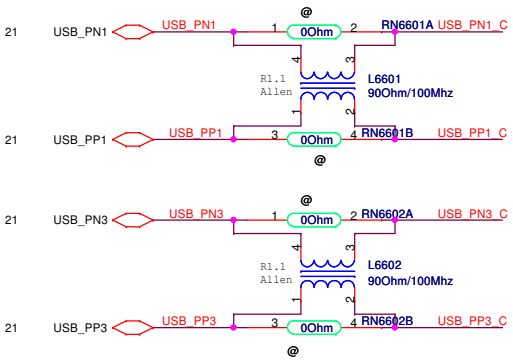


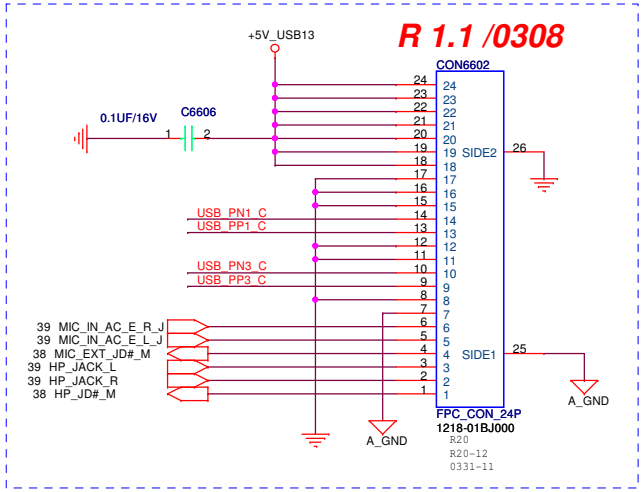
AAB70

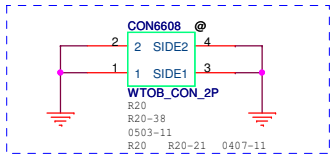
Change to High active Part





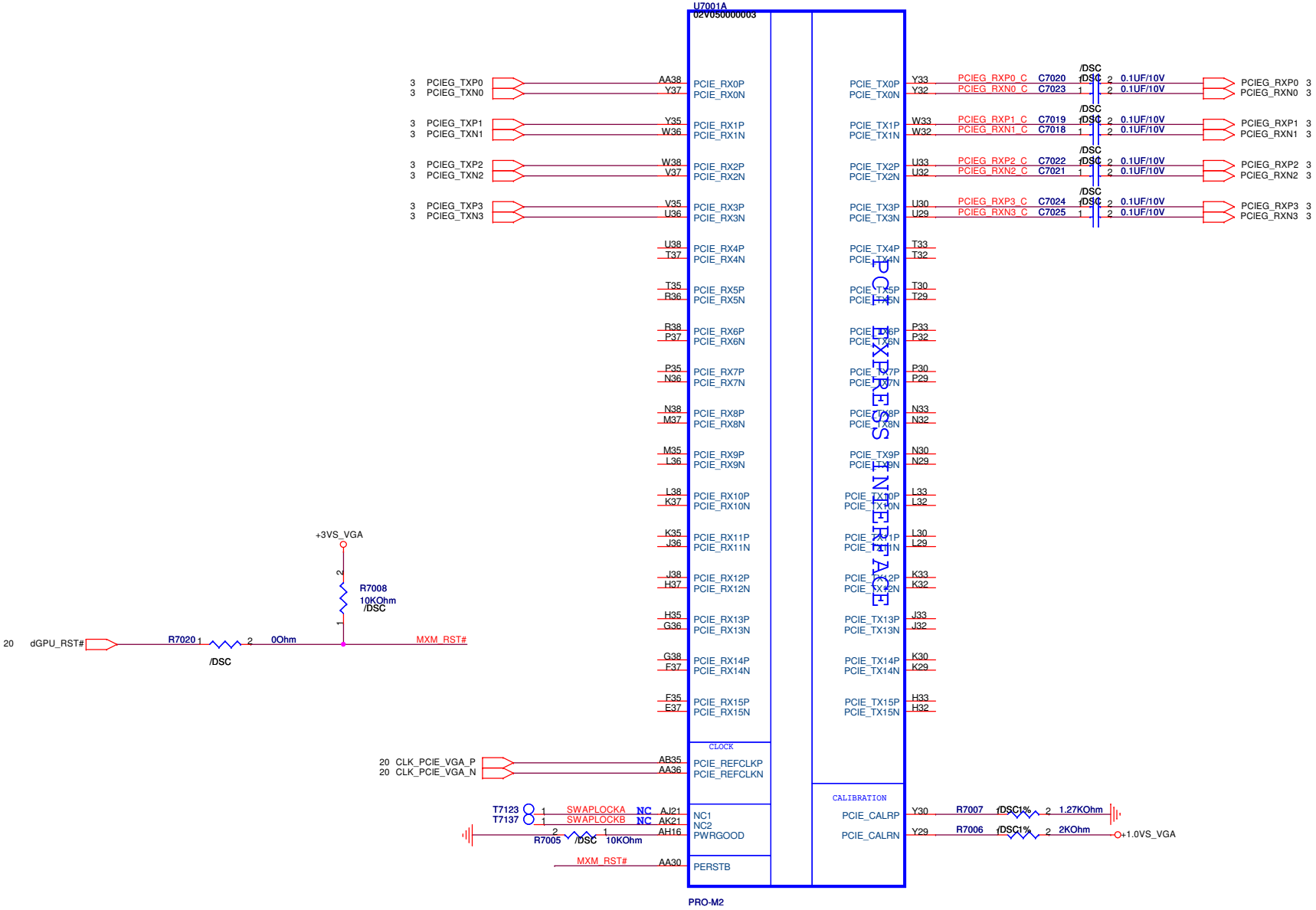




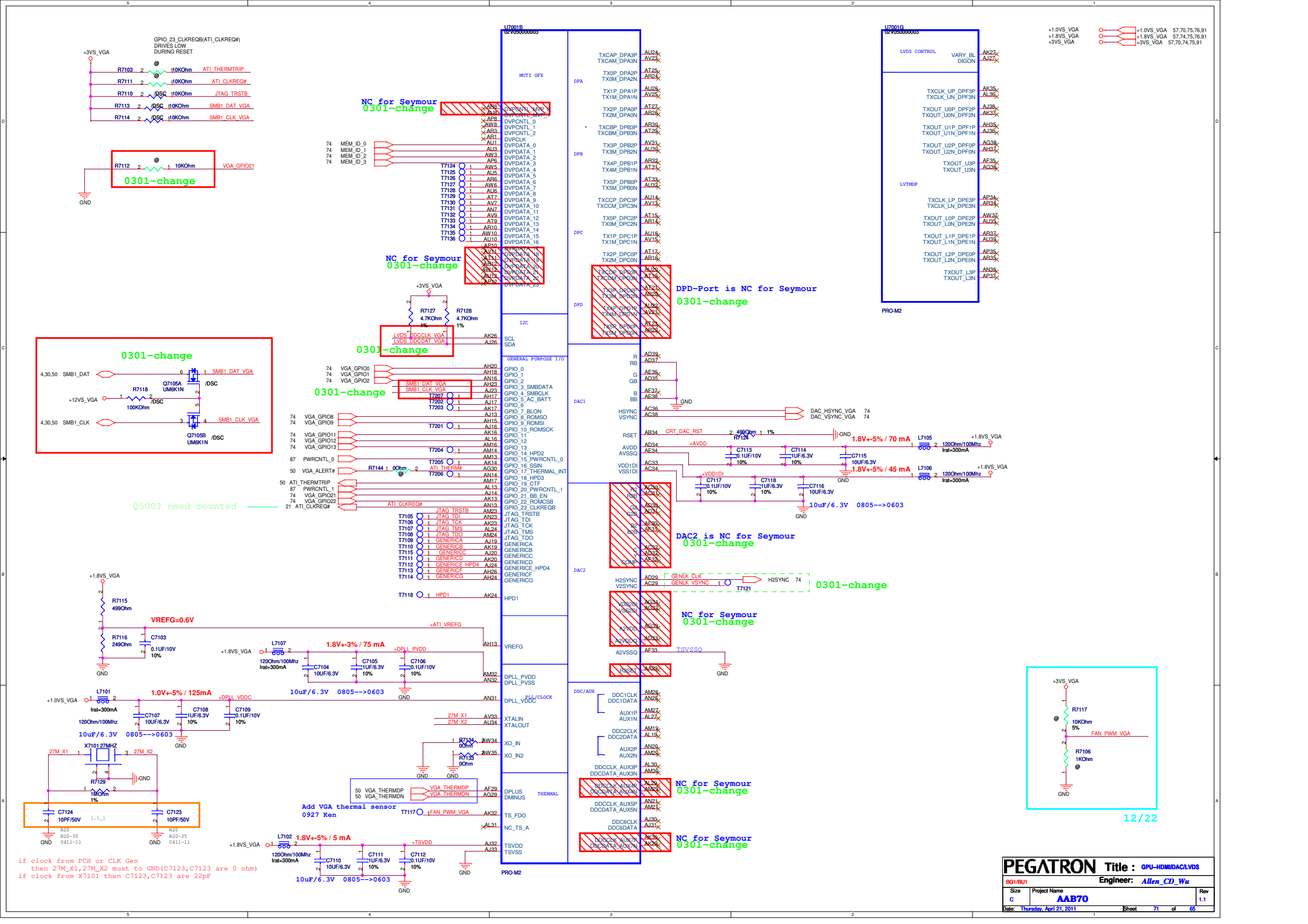


PEGATRON	Title : MDC/ PWR SW/ Debug	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Allen_CD_Wu	
Size: Custom	Project Name: AAB70	Rev: 1.1
Date: Tuesday, May 03, 2011	Sheet 66 of 99	

R 1.1 /0301 Seymour XT/M2

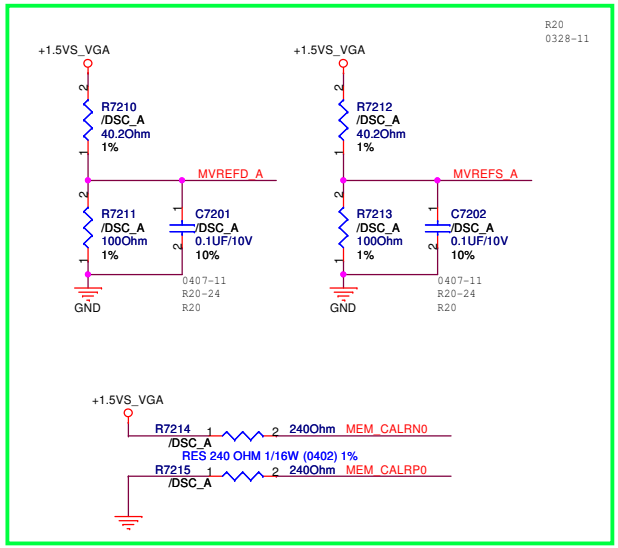


PEGATRON	Title : GPU-PCIE		
BG1/BU1	Engineer: Allen_CD_Wu		
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 70 of 99		

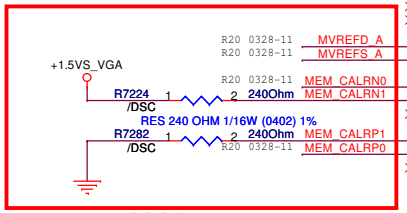

GPIO_23_CLKREQB(ATI_CLKREQ#)
DRIVES LOW
DURING RESET
+3VS_VGA
R7103 10KOhm ATI_THERMTRIP
R7111 10KOhm ATI_CLKREQ#
R7110 /DSC 10KOhm JTAG_TRSTB
R7113 /DSC 10KOhm SMB1_DAT_VGA
R7114 /DSC 10KOhm SMB1_CLK_VGA
R7112 10KOhm VGA_GPIO21
0301-change
GND
NC for Seymour
0301-change
U7001B
02V050000003
MUTI GFX
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
MEM_ID_0
MEM_ID_1
MEM_ID_2
MEM_ID_3
DPA
DPB
DPC
DPD
TXCAP_DPA3P
TXCAM_DPA3N
TX0P_DPA2P
TX0M_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N
TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N
TXCCP_DPC3P
TXCCM_DPC3N
TX0P_DPC2P
TX0M_DPC2N
TX1P_DPC1P
TX1M_DPC1N
TX2P_DPC0P
TX2M_DPC0N
TXCDP_DPD3P
TXCDM_DPD3N
TX3P_DPD2P
TX3M_DPD2N
TX4P_DPD1P
TX4M_DPD1N
TX5P_DPD0P
TX5M_DPD0N
DPD-Port is NC for Seymour
0301-change
I2C
SCL
SDA
LVDS_DDCCLK_VGA
LVDS_DDCDAT_VGA
GENERAL PURPOSE I/O
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
VGA_GPIO0
VGA_GPIO1
VGA_GPIO2
SMB1_DAT_VGA
SMB1_CLK_VGA
VGA_GPIO8
VGA_GPIO9
VGA_GPIO11
VGA_GPIO12
VGA_GPIO13
PWRCNTL_0
VGA_ALERT#
ATI_THERMTRIP
PWRCNTL_1
VGA_GPIO21
VGA_GPIO22
ATI_CLKREQ#
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF
GENERICG
HPD1
Q5003 need mounted
0301-change
DAC1
DAC2
R
RB
G
GB
B
BB
HSYNC
VSYNC
DAC_HSYNC_VGA
DAC_VSYNC_VGA
RSET
CRT_DAC_RST
AVDD
AVSSQ
VDD1DI
VSS1DI
+AVDD
+VDD1DI
1.8V+-5% / 70 mA
1.8V+-5% / 45 mA
10uF/6.3V 0805-->0603
DAC2 is NC for Seymour
0301-change
H2SYNC
V2SYNC
GENLK_CLK
GENLK_VSYNC
H2SYNC
NC for Seymour
0301-change
A2VDD
A2VSSQ
TSVSSQ
RSET
DDC/AUX
DDC1CLK
DDC1DATA
AUX1P
AUX1N
DDC2CLK
DDC2DATA
AUX2P
AUX2N
DDCCLK_AUX3P
DDCDATA_AUX3N
DDCCLK_AUX4P
DDCDATA_AUX4N
DDCCLK_AUX5P
DDCDATA_AUX5N
DDC6CLK
DDC6DATA
DDCCLK_AUX6P
DDCDATA_AUX6N
NC for Seymour
0301-change
PRO-M2
U7001G
02V050000003
LVDS CONTROL
VARY_BL
DIGON
LVTMDP
TXCLK_UP_DPF3P
TXCLK_UN_DPF3N
TXOUT_U0P_DPF2P
TXOUT_U0N_DPF2N
TXOUT_U1P_DPF1P
TXOUT_U1N_DPF1N
TXOUT_U2P_DPF0P
TXOUT_U2N_DPF0N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP_DPE3P
TXCLK_LN_DPE3N
TXOUT_L0P_DPE2P
TXOUT_L0N_DPE2N
TXOUT_L1P_DPE1P
TXOUT_L1N_DPE1N
TXOUT_L2P_DPE0P
TXOUT_L2N_DPE0N
TXOUT_L3P
TXOUT_L3N
PRO-M2
+1.0VS_VGA 57,70,75,76,91
+1.8VS_VGA 57,74,75,76,91
+3VS_VGA 57,70,74,75,91
0301-change
4,30,50 SMB1_DAT
4,30,50 SMB1_CLK
Q7105A UM6K1N
Q7105B UM6K1N
/DSC
+12VS_VGA
100KOhm
SMB1_DAT_VGA
SMB1_CLK_VGA
+1.8VS_VGA
R7115 499Ohm
VREFG=0.6V
R7116 249Ohm
C7103 0.1UF/10V 10%
+ATI_VREFG
VREFG
1.8V+-3% / 75 mA
+DPLL_PVDD
L7107 120Ohm/100Mhz Irat=300mA
C7104 10UF/6.3V
C7105 1UF/6.3V 10%
C7106 0.1UF/10V 10%
DPLL_PVDD
DPLL_PVSS
10uF/6.3V 0805-->0603
+1.0VS_VGA
L7101 Irat=300mA
1.0V+-5% / 125mA
+DPLL_VDDC
C7107 10UF/6.3V
C7108 1UF/6.3V 10%
C7109 0.1UF/10V 10%
120Ohm/100Mhz
10uF/6.3V 0805-->0603
DPLL_VDDC
PLL/CLOCK
27M_X1
27M_X2
XTALIN
XTALOUT
X7101 27MHZ
R7129 1MOhm 1%
C7124 10PF/50V
C7123 10PF/50V
R20-35 0411-11
XO_IN
XO_IN2
R7134 0Ohm
R7135 0Ohm
Add VGA thermal sensor
0927 Ken
VGA_THERMDP
VGA_THERMDN
DPLUS
DMINUS
THERMAL
FAN_PWM_VGA
TS_FDO
NC_TS_A
L7102 120Ohm/100Mhz Irat=300mA
1.8V+-5% / 5 mA
+TSVDD
C7110 10UF/6.3V
C7111 1UF/6.3V 10%
C7112 0.1UF/10V 10%
10uF/6.3V 0805-->0603
TSVDD
TSVSS
if clock from PCH or CLK Gen
then 27M_X1,27M_X2 must to GND(C7123,C7123 are 0 ohm)
if clock from X7101 then C7123,C7123 are 22pF
+3VS_VGA
R7117 10KOhm 5%
FAN_PWM_VGA
R7106 1KOhm
12/22
PEGATRON
Title : GPU-HDMI/DAC/LVDS
BG1/BU1
Engineer: Allen_CD_Wu
Size C
Project Name AAB70
Rev 1.1
Date: Thursday, April 21, 2011
Sheet 71 of 65

The all balls are NC except N12 /M12 for seymour

Reserve,Unmount



The all balls are NC except N12 /M12 for seymour



0301-change

U7001C 02V050000003

MEMORY INTERFACE A

	DDR2 GDDR3/GDDR5 DDR3		DDR2 GDDR5/GDDR3 DDR3
C37	DQA0_0	MAA0_0	G24
C35	DQA0_1	MAA0_1	J23
A35	DQA0_2	MAA0_2	H24
E34	DQA0_3	MAA0_3	J24
G32	DQA0_4	MAA0_4	H26
D33	DQA0_5	MAA0_5	J26
F32	DQA0_6	MAA0_6	H21
E32	DQA0_7	MAA0_7	G21
D31	DQA0_8	MAA1_0	H19
F30	DQA0_9	MAA1_1	H20
C30	DQA0_10	MAA1_2	L13
A30	DQA0_11	MAA1_3	G16
F28	DQA0_12	MAA1_4	J16
C28	DQA0_13	MAA1_5	H16
A28	DQA0_14	MAA1_6	J17
E28	DQA0_15	MAA1_7	H17
D27	DQA0_16		
F26	DQA0_17	WCKA0_0	A32
C26	DQA0_18	WCKA0B_0	C32
A26	DQA0_19	WCKA0_1	D23
F24	DQA0_20	WCKA0B_1	F22
C24	DQA0_21	WCKA1_0	C14
A24	DQA0_22	WCKA1B_0	A14
E24	DQA0_23	WCKA1_1	E10
C22	DQA0_24	WCKA1B_1	D9
A22	DQA0_25	GDDR5/DDR2/GDDR3	
F22	DQA0_26	EDCA0_0	C34
D21	DQA0_27	EDCA0_1	D29
A20	DQA0_28	EDCA0_2	D25
F20	DQA0_29	EDCA0_3	E20
D19	DQA0_30	EDCA1_0	E16
E18	DQA0_31	EDCA1_1	E12
C18	DQA1_0	EDCA1_2	J10
A18	DQA1_1	EDCA1_3	D7
F18	DQA1_2		
D17	DQA1_3	DDBIA0_0	A34
A16	DQA1_4	DDBIA0_1	E30
F16	DQA1_5	DDBIA0_2	E26
D15	DQA1_6	DDBIA0_3	C20
E14	DQA1_7	DDBIA1_0	C16
F14	DQA1_8	DDBIA1_1	C12
D13	DQA1_9	DDBIA1_2	J11
F12	DQA1_10	DDBIA1_3	F8
A12	DQA1_11		
D11	DQA1_12	ADBIA0	J21
F10	DQA1_13	ADBIA1	G19
A10	DQA1_14		
C10	DQA1_15	CLKA0	H27
G13	DQA1_16	CLKA0B	G27
H13	DQA1_17		
J13	DQA1_18	CLKA1	J14
H11	DQA1_19	CLKA1B	H14
G10	DQA1_20		
G8	DQA1_21	RASA0B	K23
K9	DQA1_22	RASA1B	K19
K10	DQA1_23		
G9	DQA1_24	CASA0B	K20
A8	DQA1_25	CASA1B	K17
C8	DQA1_26		
E8	DQA1_27	CSA0B_0	K24
A6	DQA1_28	CSA0B_1	K27
C6	DQA1_29		
E6	DQA1_30	CSA1B_0	M13
A5	DQA1_31	CSA1B_1	K16
	MVREFDA	CKEA0	K21
	MVREFSA	CKEA1	J20
	MEM_CALRN0	WEA0B	K26
	MEM_CALRN1	WEA1B	L15
AG12	MEM_CALRN2		
	MEM_CALRP1	MAA0_8	H23
M27	MEM_CALRP0	MAA1_8	J19
AH12	MEM_CALRP2	GDDR5	

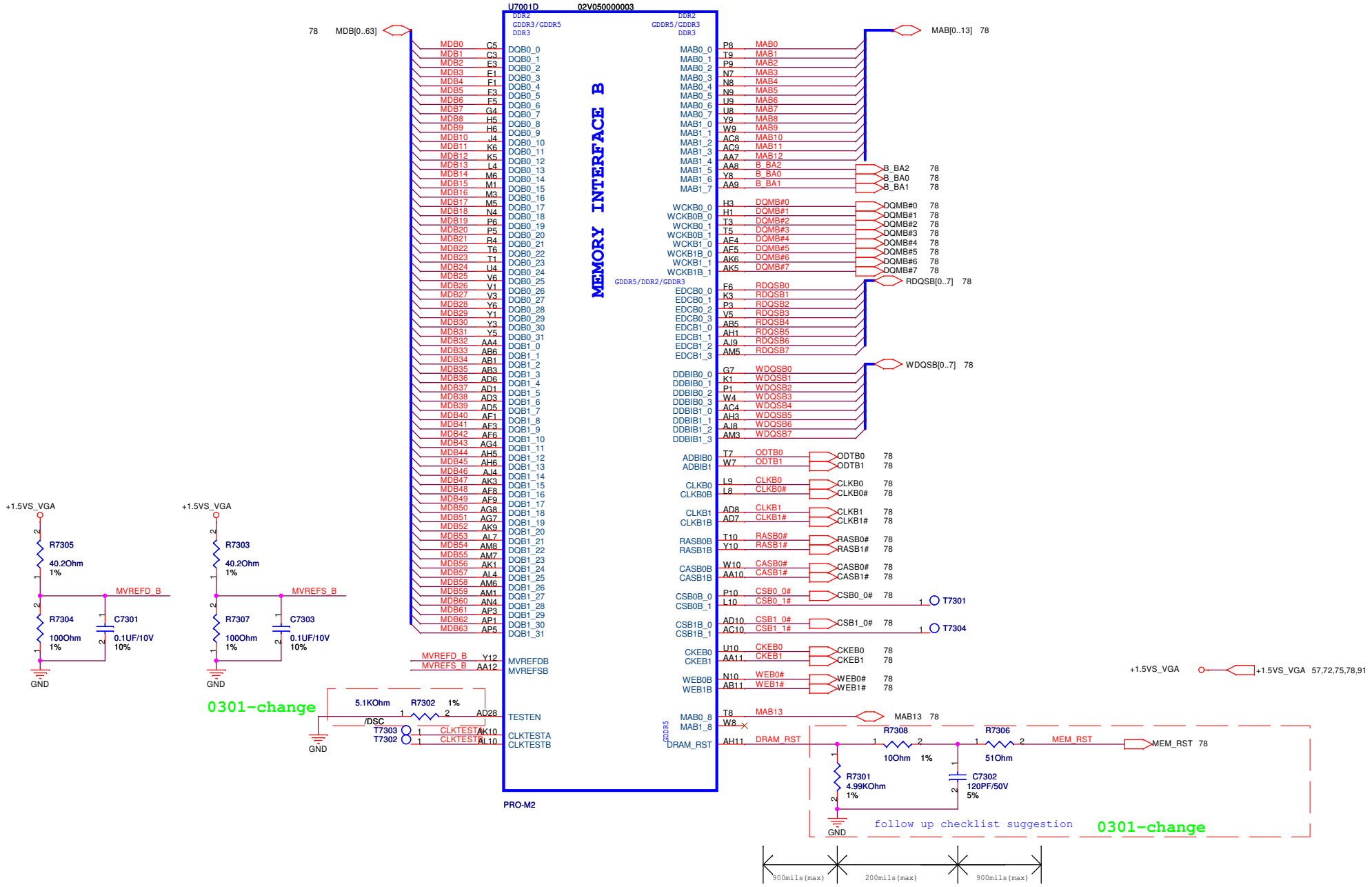
PRO-M2

PEGATRON Title : GPU-MEM_CTRL_CHA

BG1/BU1 Engineer: Allen_CD_Wu

Size	Project Name	Rev
Custom	AAB70	1.1

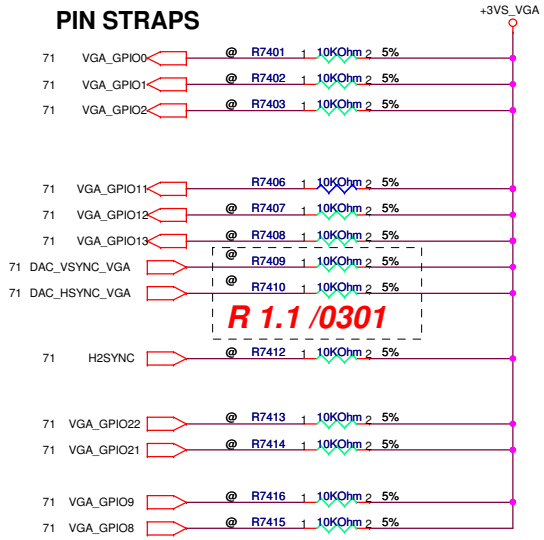
Date: Thursday, April 07, 2011 Sheet 72 of 99



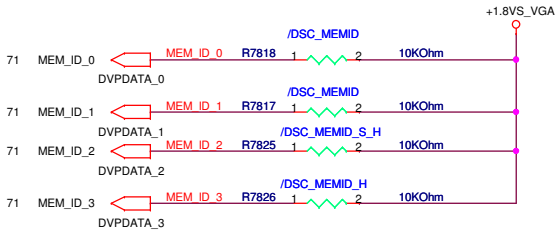
PEGATRON	Title : GPU-MEM_CTRL_CHB		
BG1/BU1	Engineer: Allen_CD_Wu		
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 73 of 99		

GPIO21 MUST BE LOW DURING PERSTB WHEN BEING USED TO CONTROL MVDDQ

PIN STRAPS



VRAM size define by VBIOS



Seymour Straps

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled MXM and add-in boards	0 (internal pull-down)
BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1,then Config[2:0]defines the ROM type. If BIOS_ROM_EN=0,then Config[2:0]deifnes the primary memoru apeture size. 128MB---000 32MB---Not Support 2GB---Not Support 256MB---001 512MB--Not Support 4GB---Not Support 64MB----010 1GB-----Not Support	0000 (internal pull-down)
BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI.	0 (internal pull-down)
Reserved	GENLK_CLK GPIO_21_BB_EN GPIO8	ATI internal use only . THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)

Seymour XT:

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR3 Memory Type	VRAM Vendor Part
Hynix	0000	0	64M*16*4 pcs(512MB)	H5TQ1G63BFR-12 (1600Mbps)
	0001	1	64M*16*4 pcs(512MB)	H5TQ1G63DFR-12C (1600Mbps)
	0010	2	128M*16*4 pcs(1GB)	H5TQ2G63BFR-12C (1600Mbps)
	0011	3	128M*16*4 pcs(1GB)	H5TQ2G63BFR-11C LF (1600Mbps)
	0100	4		
	0101	5		
	0110	6		
	0111	7		
Samsung	1000	8	64M*16*4 pcs(512MB)	K4W1G1646E-HC12 (1600Mbps)
	1001	9	64M*16*4 pcs(512MB)	K4W1G1646G-BC12 (1600Mbps)
	1010	10	128M*16*4 pcs(1GB)	K4W2G1646B-HC12 (1600Mbps)
	1011	11	128M*16*4 pcs(1GB)	K4W2G1646C-HC12 (1600Mbps)
	1100	12		
	1101	13		
	1110	14		
	1111	15		

PEGATRON Title : GPU-STRAP_MISC

BG1/BU1 Engineer: Allen_CD_Wu

Size: Custom | Project Name: AAB70 | Rev: 1.1

Date: Thursday, April 21, 2011 | Sheet 74 of 99

R 1.1 /0301

Capilano/ Whistler : 1.5V DC+-3% / 3.4A Peak

Capilano: 1.8V DC+-3% / 17 mA, Whistler: TBD

Capilano: 3.3V DC+-3% / 60 mA, Whistler : TBD

Capilano: 1.8V DC+-3% / 170 mA, Whistler : TBD

Capilano/ Whistler: 1.8V DC+-5% / 40mA

Add Bead L7504
0927 Ken

Capilano/ Whistler: 1.8V DC+-5% / 150mA

Capilano/ Whistler: 1.8V DC+-3% / 50mA

Capilano/ Whistler: 1.0V DC+-3% / 100mA

Capilano/ Whistler: PCIE _VDDR 1.8V+-3% / 400mA

Capilano/ Whistler: PCIE_VDDC 1.0V DC+-3% / 1.1A

Capilano: VDDC+VDDCI +-3% / 27.6A, Whistler: TBD

Capilano: VDDC+VDDCI +-3% / 27.6A, Whistler: TBD

Reduce 10u*2,1u*4 for cost saving

Reduce 10u for cost saving

Reduce 10u,1u*3 for cost saving

Reduce 1u *2 for cost saving

Reduce 10u*8,1u *8 for cost saving

Reduce 1u *4 for cost saving

10uF/6.3V 0805-->0603

PX_EN=0: Normal Operation
PX_EN=1: BACO Mode

BIF short with +VDDC_VGA if BACO is not support
BIF_VDDC: I=55mA@BACO MODE (AN_MGEN_R5)

NC for seymour

GND

POWER

R 1.1 /0301

R 1.1 /0301

R 1.1 /0301

R 1.1 /0301

R 1.1 /0301

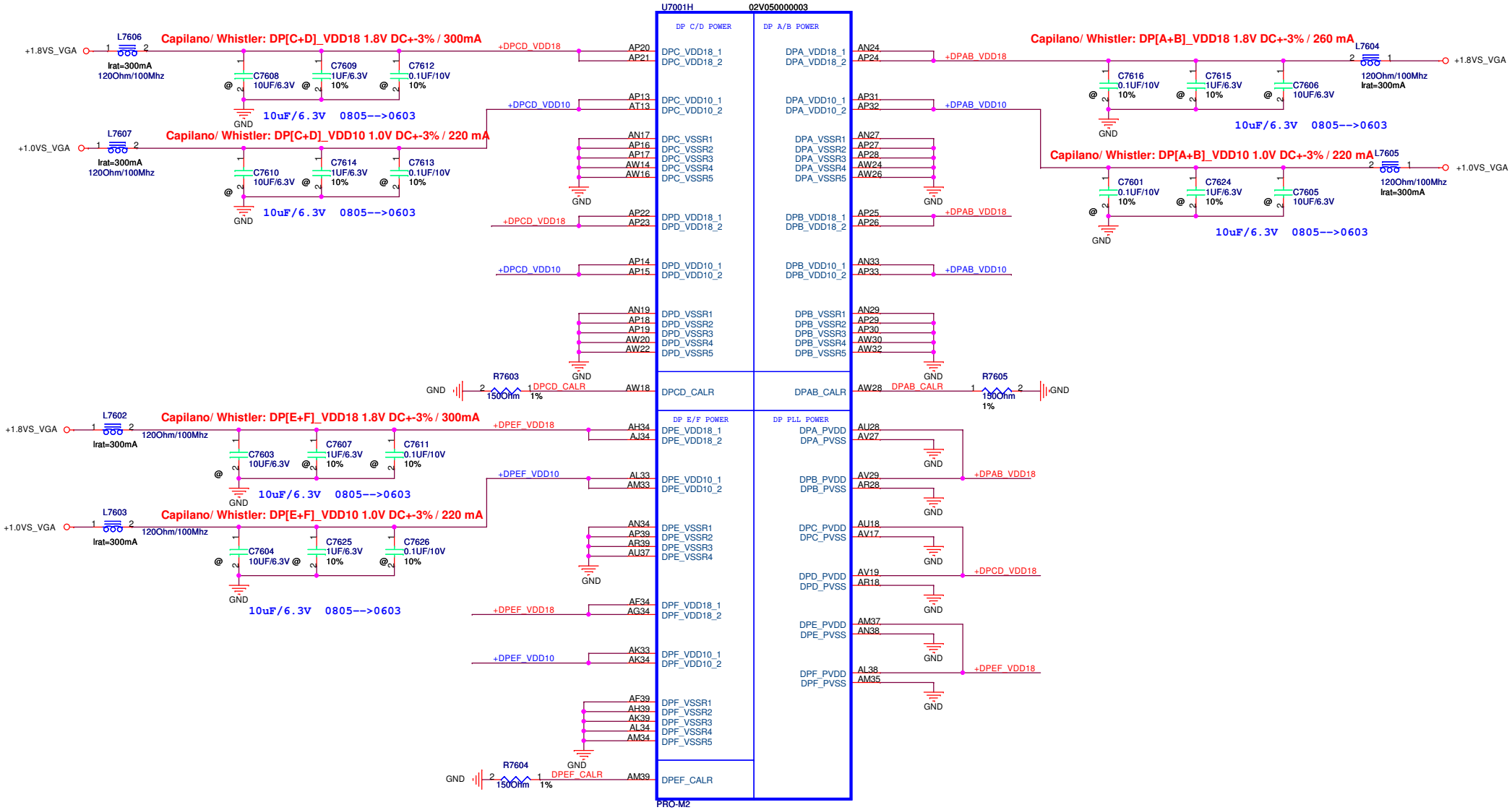
20 mil

PEGATRON	Title :	(N)GPU-POWER(MD	
BG1/BU1	Engineer:	Allen_CD_Wu	
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 75 of 99		

+1.0VS_VGA
+1.8VS_VGA
+1.0VS_VGA 57,70,71,75,91
+1.8VS_VGA 57,71,74,75,91

0301-change

PX with BACO mode all displays are always driven by APU
DPA&DPB share power ;DPC&DPD share power ;DPE&DPF share power



PEGATRON	Title :	(2)GPU-DP POWER	
BG1/BU1	Engineer:	Allen_CD_Wu	
Size: Custom	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 76 of 99		

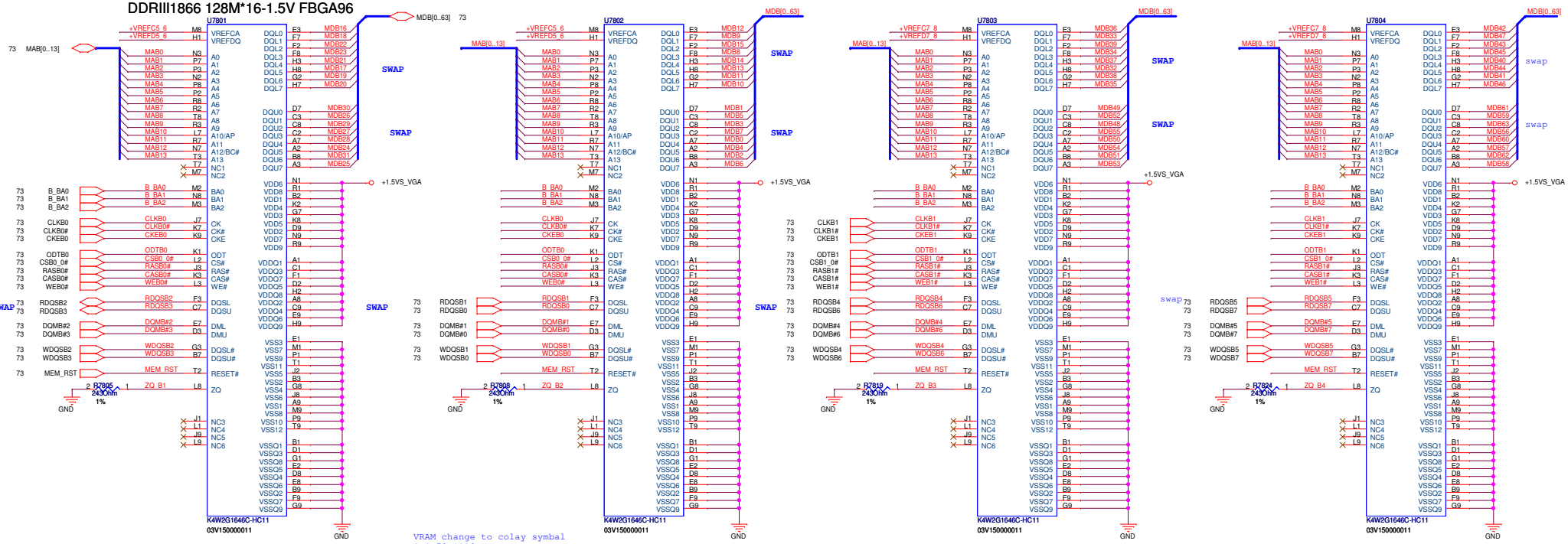
PEGATRON Title : GPU-MEM CHA

BG1/BU1 Engineer: Allen_CD_Wu

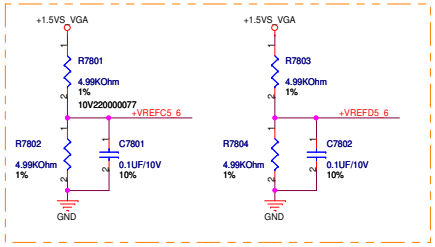
Size	Project Name	Rev
C	AAB70	1.1

Date: Monday, March 21, 2011 Sheet 77 of 99

DDRIII1866 128M*16-1.5V FBGA96

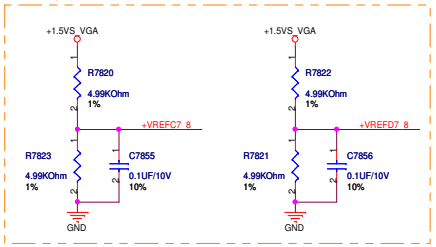


U7801,U7802 share a Verf

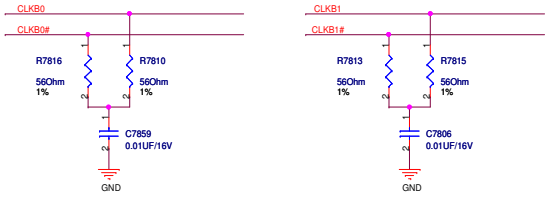


cost saving

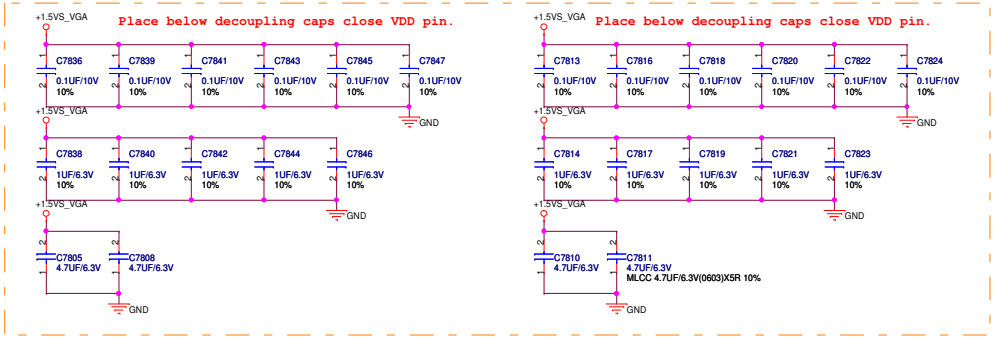
U7803,U7804 share a Verf



cost saving

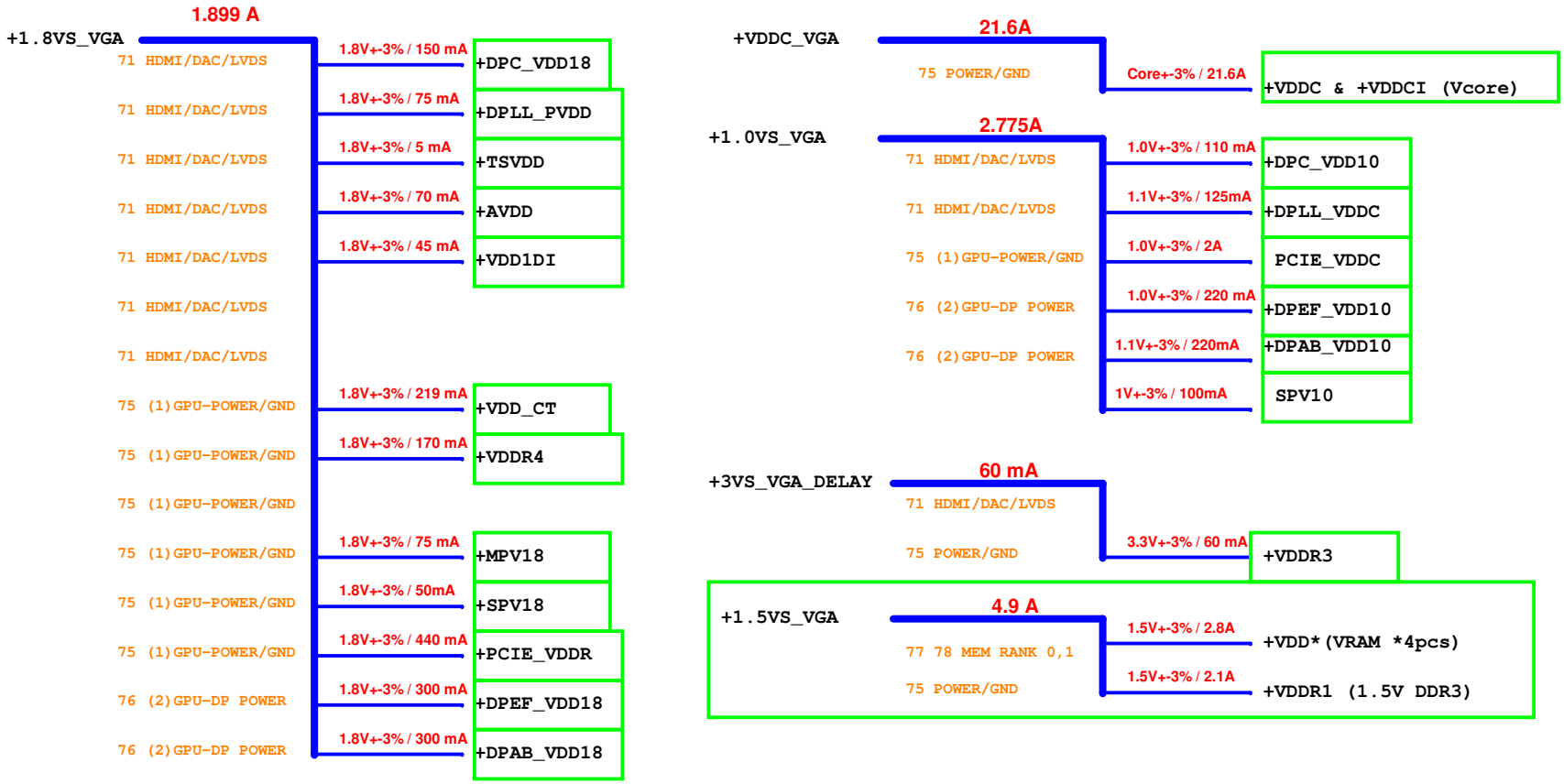


7.5uF per one VRAM



+1.5VS_VGA +1.5VS_VGA 57,72,73,75,91

PEGATRON	Title : GPU-MEM CHB		
BG1/BU1	Engineer: Allen_CD_Wu		
Size: C	Project Name: AAB70		Rev: 1.1
Date: Thursday, April 21, 2011	Sheet 78 of 99		



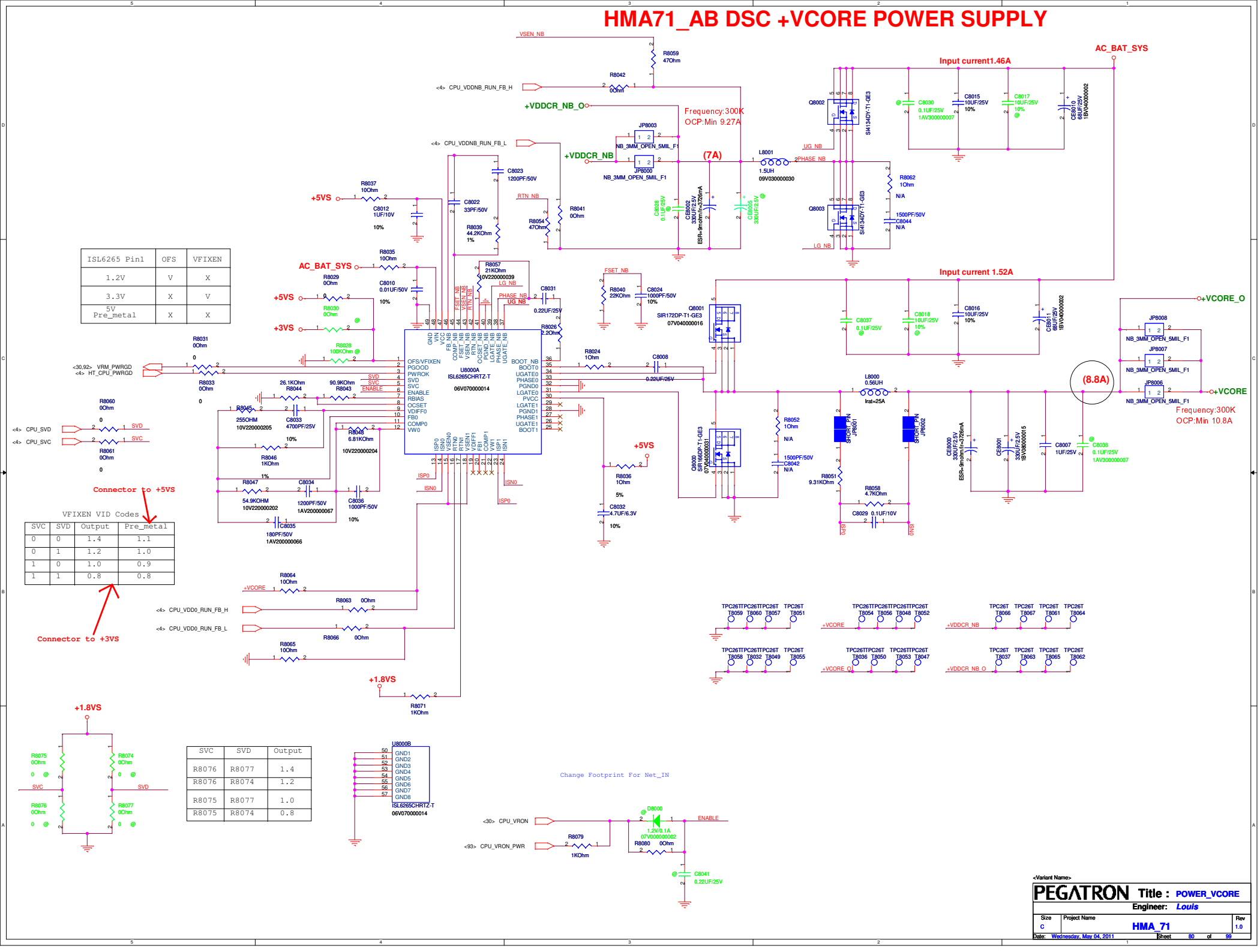
Total:15W (w/o VRAM)

Power Up Sequence :
+VGA_VCORE -> +1.05VS_VGA -> +1.5VS_VGA -> +1.8VS_VGA -> +3VS_VGA_DELAY

Power Down Sequence :
+3VS_VGA_DELAY -> +1.8VS_VGA -> +1.5VS_VGA -> +1.05VS_VGA -> +VGA_VCORE

PEGATRON	Title : ATI_Robson	
<OrgName>	Engineer: Allen_CD_Wu	
Size: Custom	Project Name: AAB70	Rev: 1.1
Date: Monday, March 21, 2011	Sheet 79 of 99	

HMA71_AB DSC +VCORE POWER SUPPLY



<Variant Name>

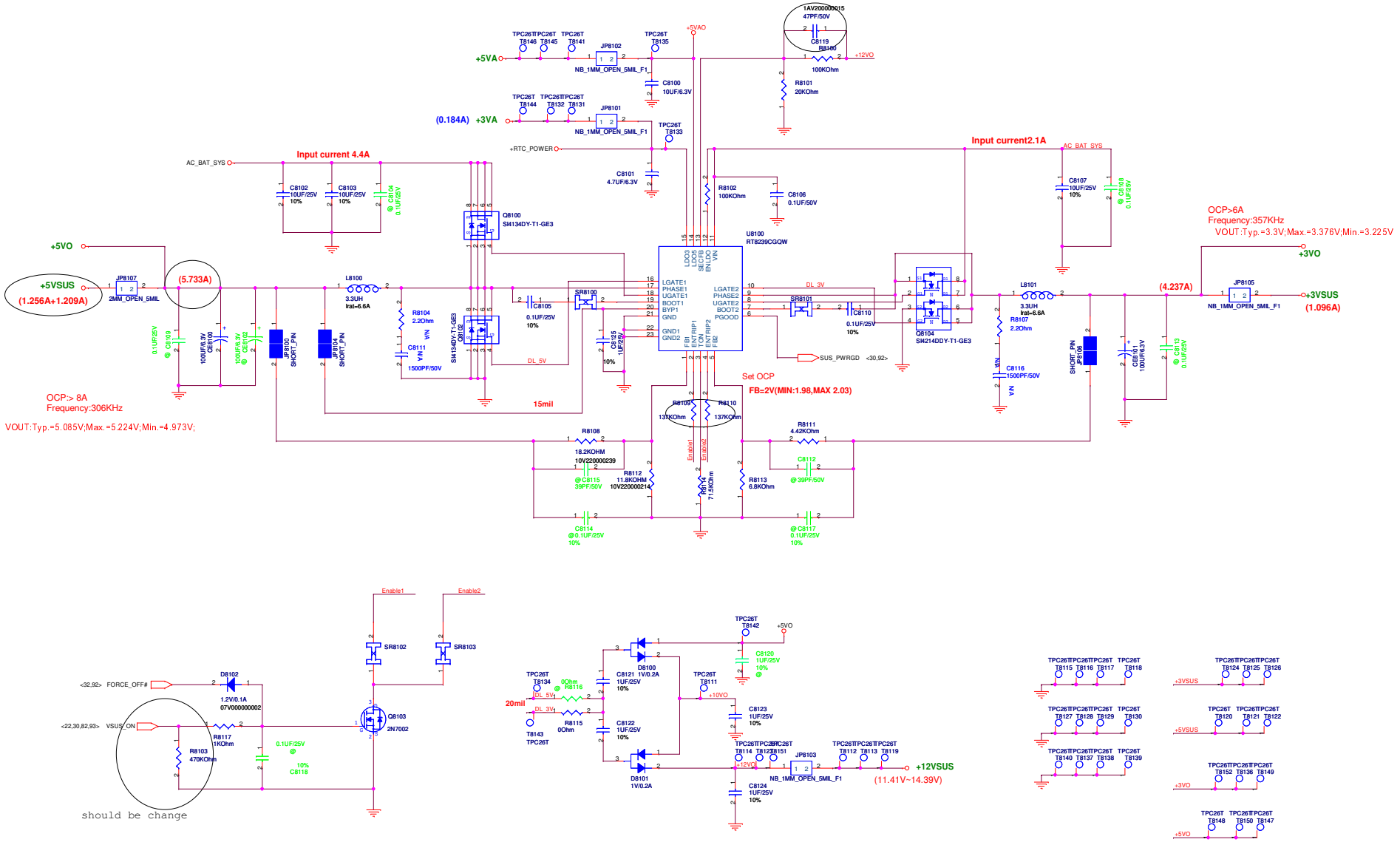
PEGATRON Title : POWER_VCORE

Engineer: Louis

Size	Project Name	Rev
C	HMA_71	1.0

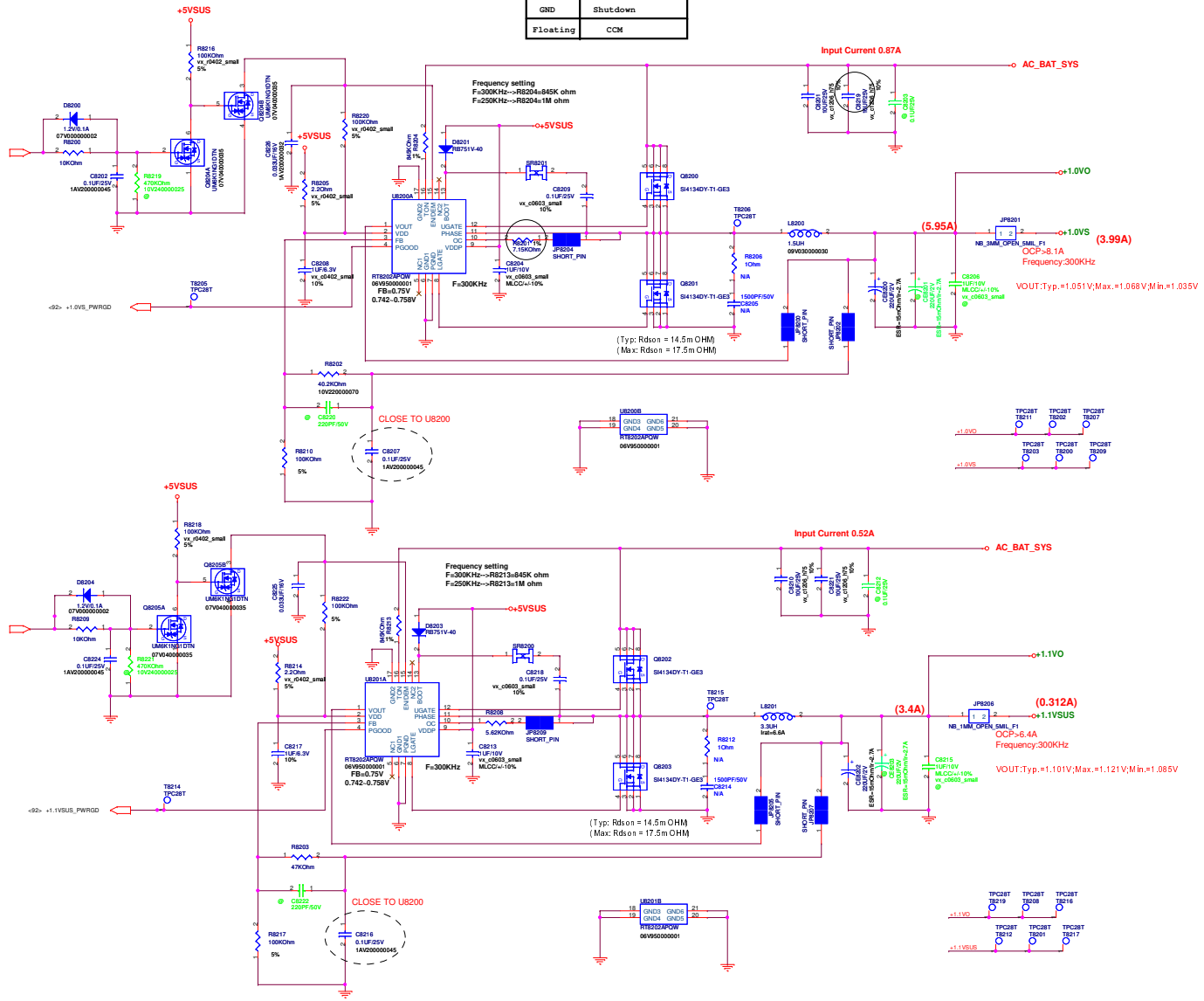
Date: Wednesday, May 04, 2011 Sheet 80 of 99

HMA71 DSC +SYSTEM POWER SUPPLY



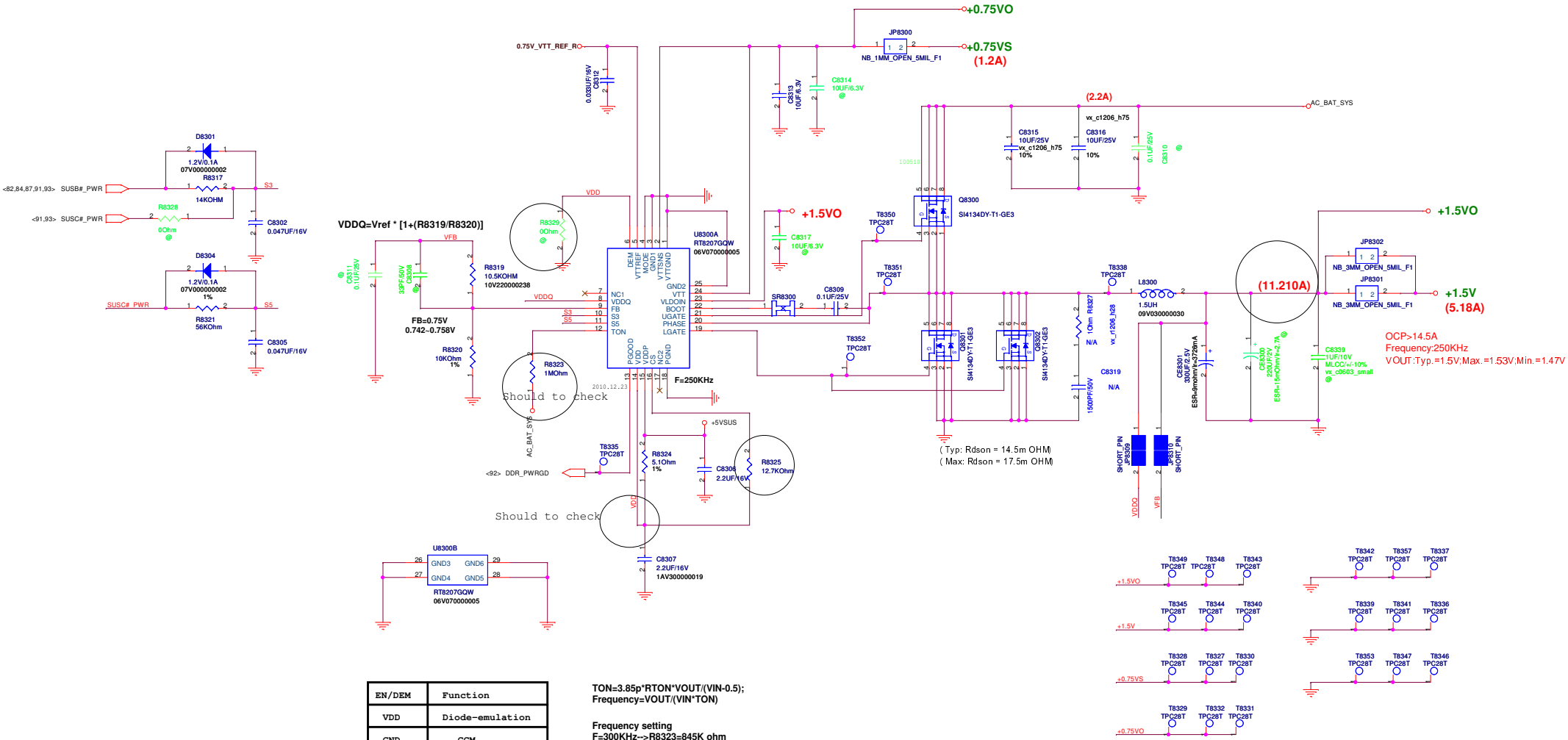
HMA71 DSC +1.0VO&+1.1VO POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



PEGATRON	Title :	POWER_+1.1V & +1.0V	
<OrgName>	Engineer:	Louis	
Size: Custom	Project Name: HMA71		Rev: 1.0
Date: Wednesday, May 04, 2011	Sheet 82 of 99		

+1.5VO & +0.75VS POWER SUPPLY



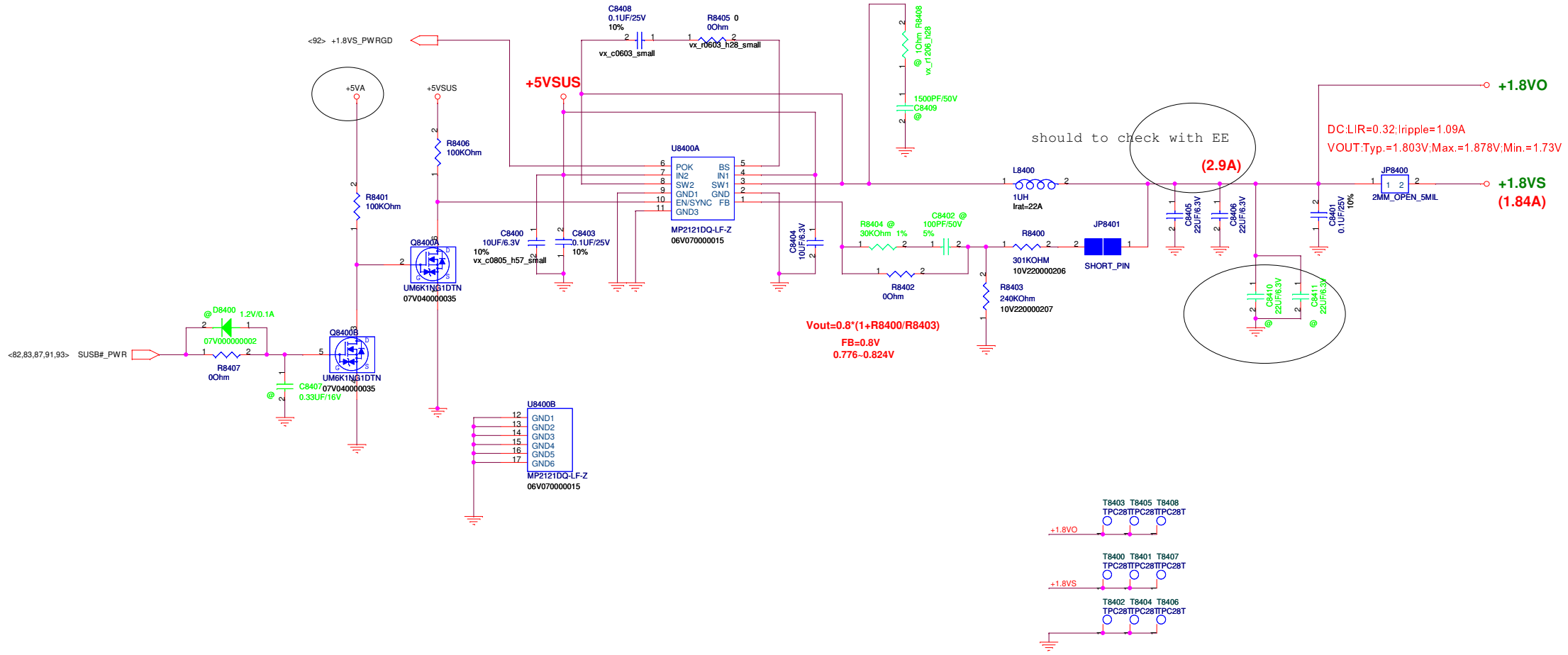
EN/DEM	Function
VDD	Diode-emulation
GND	CCM

TON=3.85p*RTON*VOUT/(VIN-0.5);
Frequency=VOUT/(VIN*TON)

Frequency setting
F=300KHz-->R8323=845K ohm
F=250KHz-->R8323=1M ohm

PEGATRON Title : POWER_DDR & VTT
<OrgName> Engineer: Louis
Size: Custom | Project Name: HMA71 | Rev: 1.0
Date: Wednesday, May 04, 2011 | Sheet 83 of 99

+1.8VS POWER SUPPLY



PEGATRON Title : POWER_+1.8VS

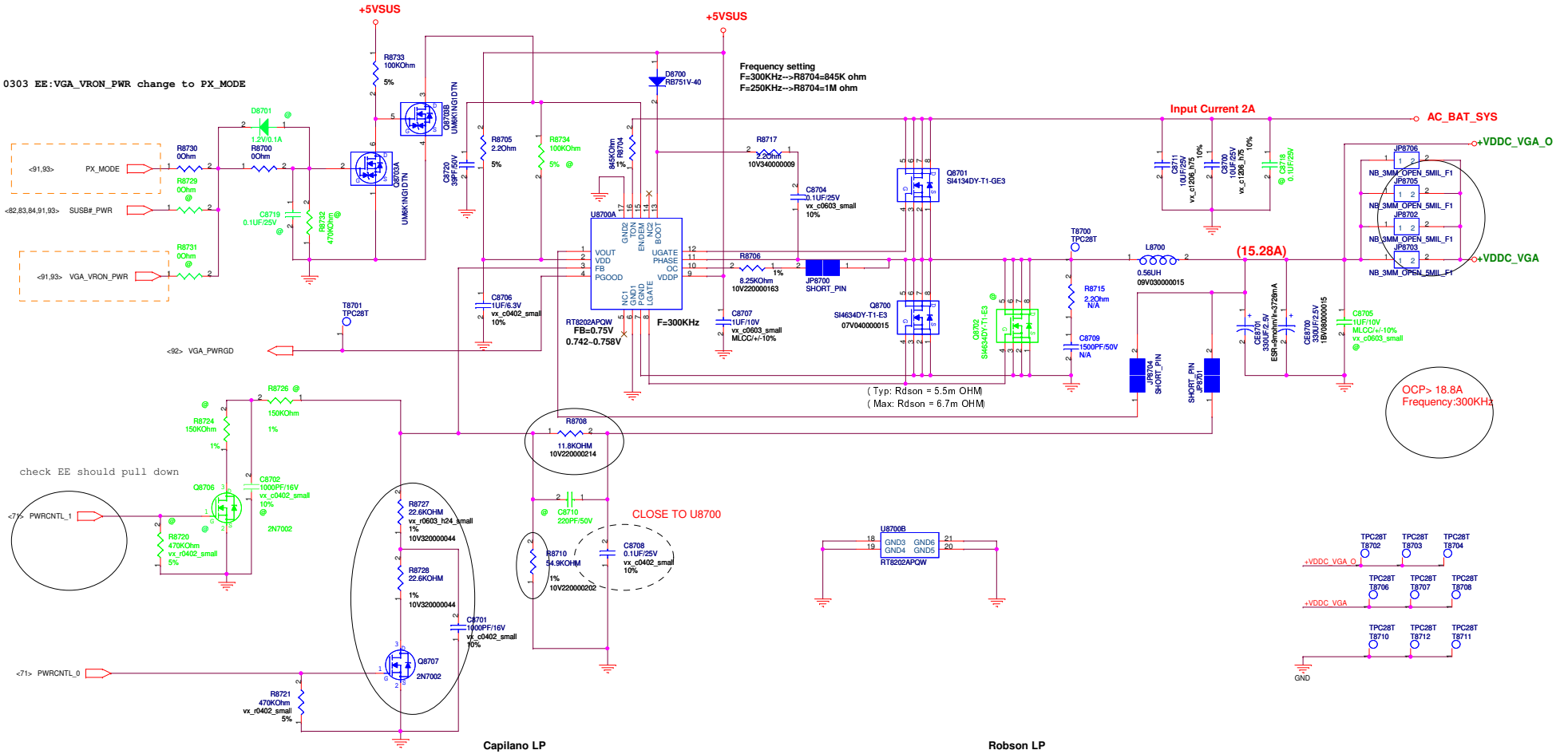
<OrgName> Engineer: Louis

Size	Project Name	Rev
Custom		1.0

Date: Wednesday, May 04, 2011 Sheet 84 of 99

AAB70 DSC +VGA_VCORE POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



Seymour XT (17W)

PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORE
LOW	LOW	0.9V/real 0.911V
LOW	HIGH	1.1V / real1.107V

Capilano LP

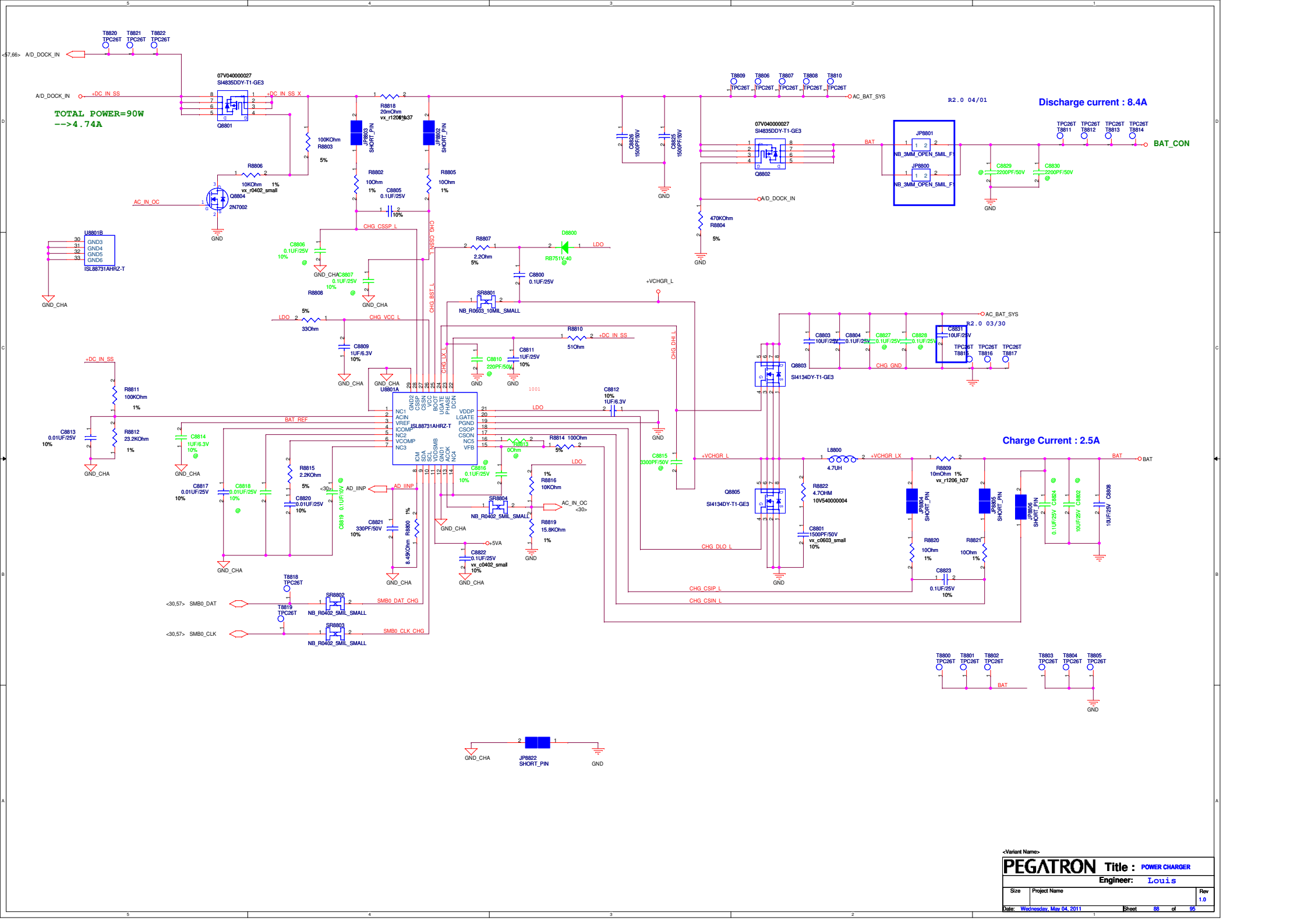
PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORE
LOW	LOW	1V
LOW	HIGH	0.9V
HIGH	HIGH	0.95V

R8727=75K ohm
R8728=75K ohm
R8726, R8724, R8720, Q8708 must be mounted.

Robson LP

PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORE
LOW	LOW	0.95V
LOW	HIGH	0.9V

PEGATRON Title : PWR_+VDDC_VGA
<OrgName> Engineer: Louis
Size: C | Project Name: HAM71 | Rev: 1.0
Date: Wednesday, May 04, 2011 | Sheet 87 of 99


TOTAL POWER=90W
-->4.74A
Discharge current : 8.4A
Charge Current : 2.5A
R2.0 04/01
R2.0 03/30
BAT_CON
ISL88731AHRZ-T
U8801A
U8801B
Q8801
Q8802
Q8803
Q8804
Q8805
2N7002
SI4835DDY-T1-GE3
SI4134DY-T1-GE3
07V040000027
A/D_DOCK_IN
AC_BAT_SYS
+DC_IN_SS
+VCHGR_L
+VCHGR_LX
CHG_CSSP_L
CHG_BST_L
CHG_VCC_L
CHG_DHI_L
CHG_DLO_L
CHG_CSIP_L
CHG_CSIN_L
BAT_REF
AD_IINP
AC_IN_OC
SMB0_DAT_CHG
SMB0_CLK_CHG
R8818 20mOhm vx_r1206_h37
R8809 10mOhm 1% vx_r1206_h37
L8800 4.7UH
R8822 4.7OHM 10V540000004
C8801 1500PF/50V vx_c0603_small
C8822 0.1UF/25V vx_c0402_small
R8819 15.8KOhm 1%
R8816 10KOhm 1%
R8815 2.2KOhm 5%
R8811 100KOhm 1%
R8812 23.2KOhm 1%
R8813 0Ohm
R8814 100Ohm 5%
R8810 51Ohm
R8807 2.2Ohm 5%
R8806 10KOhm 1% vx_r0402_small
R8803 100KOhm 5%
R8804 470KOhm 5%
R8802 10Ohm 1%
R8805 10Ohm 1%
R8820 10Ohm 1%
R8821 10Ohm 1%
C8823 0.1UF/25V 10%
C8821 330PF/50V 10%
C8819 0.1UF/10V
C8820 0.01UF/25V 10%
C8817 0.01UF/25V 10%
C8818 0.01UF/25V 10%
C8813 0.01UF/25V 10%
C8814 1UF/6.3V 10%
C8809 1UF/6.3V 10%
C8812 1UF/6.3V 10%
C8811 1UF/25V 10%
C8810 220PF/50V
C8816 0.1UF/25V 10%
C8815 3300PF/50V
C8806 0.1UF/25V 10%
C8807 0.1UF/25V 10%
C8800 0.1UF/25V
C8826 1500PF/50V
C8825 1500PF/50V
C8829 2200PF/50V
C8830 2200PF/50V
C8803 10UF/25V
C8804 0.1UF/25V
C8827 0.1UF/25V
C8828 0.1UF/25V
C8831 10UF/25V
C8824 0.1UF/25V
C8832 10UF/25V
C8808 10UF/25V
C8805 0.1UF/25V
SR8801 NB_R0603_10MIL_SMALL
SR8802 NB_R0402_5MIL_SMALL
SR8803 NB_R0402_5MIL_SMALL
SR8804 NB_R0402_5MIL_SMALL
D8800 RB751V-40
JP8801 NB_3MM_OPEN_5MIL_F
JP8800 NB_3MM_OPEN_5MIL_F
JP8803 SHORT_PIN
JP8802 SHORT_PIN
JP8804 SHORT_PIN
JP8805 SHORT_PIN
JP8806 SHORT_PIN
JP8822 SHORT_PIN
T8820 TPC26T
T8821 TPC26T
T8822 TPC26T
T8809 TPC26T
T8806 TPC26T
T8807 TPC26T
T8808 TPC26T
T8810 TPC26T
T8811 TPC26T
T8812 TPC26T
T8813 TPC26T
T8814 TPC26T
T8815 TPC26T
T8816 TPC26T
T8817 TPC26T
T8818 TPC26T
T8819 TPC26T
T8800 TPC26T
T8801 TPC26T
T8802 TPC26T
T8803 TPC26T
T8804 TPC26T
T8805 TPC26T
<57,66> A/D_DOCK_IN
<30,57> SMB0_DAT
<30,57> SMB0_CLK
GND
GND_CHA
LDO
+5VA
PEGATRON
Title : POWER CHARGER
Engineer: Louis
Size
Project Name
Rev 1.0
Date: Wednesday, May 04, 2011
Sheet 88 of 95

BATTERY IN DETECT

<Variant Name>

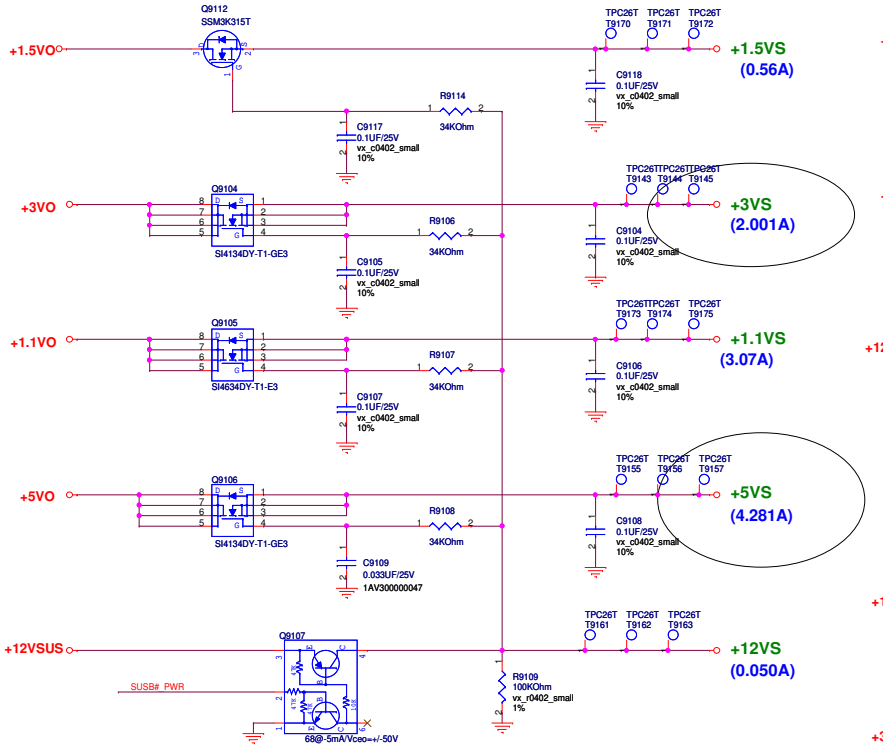
PEGATRON Title : POWER_DETECT

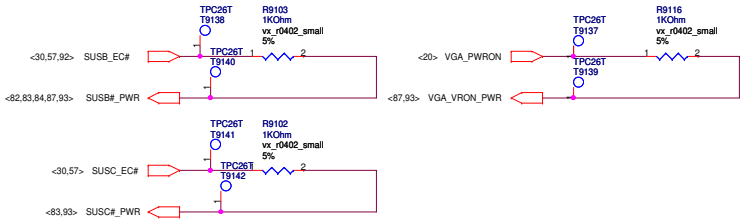
Engineer: Louis

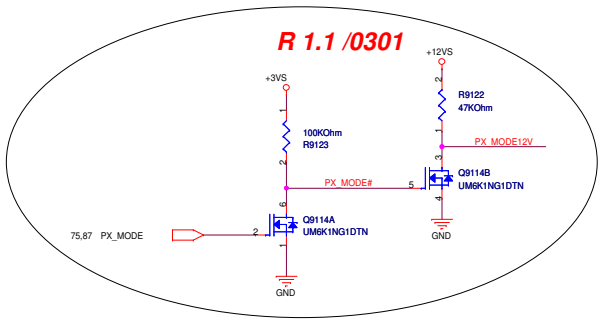
Size	Project Name	Rev
Custom		1.0

Date: Wednesday, May 04, 2011 Sheet 90 of 99

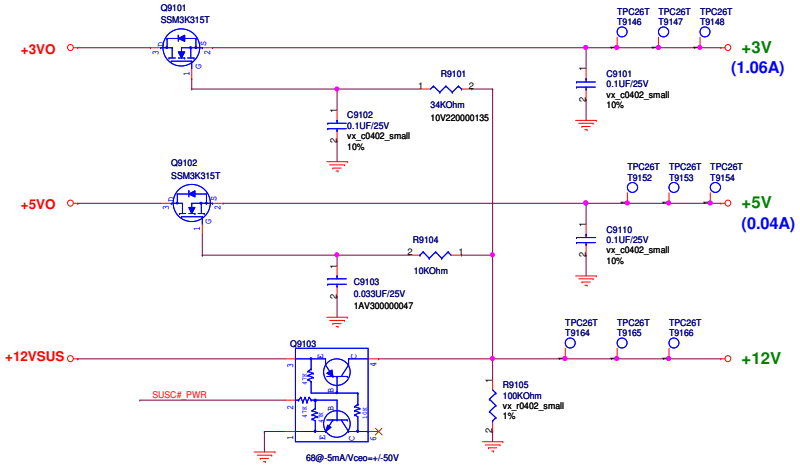
SUSB#_PWR POWER



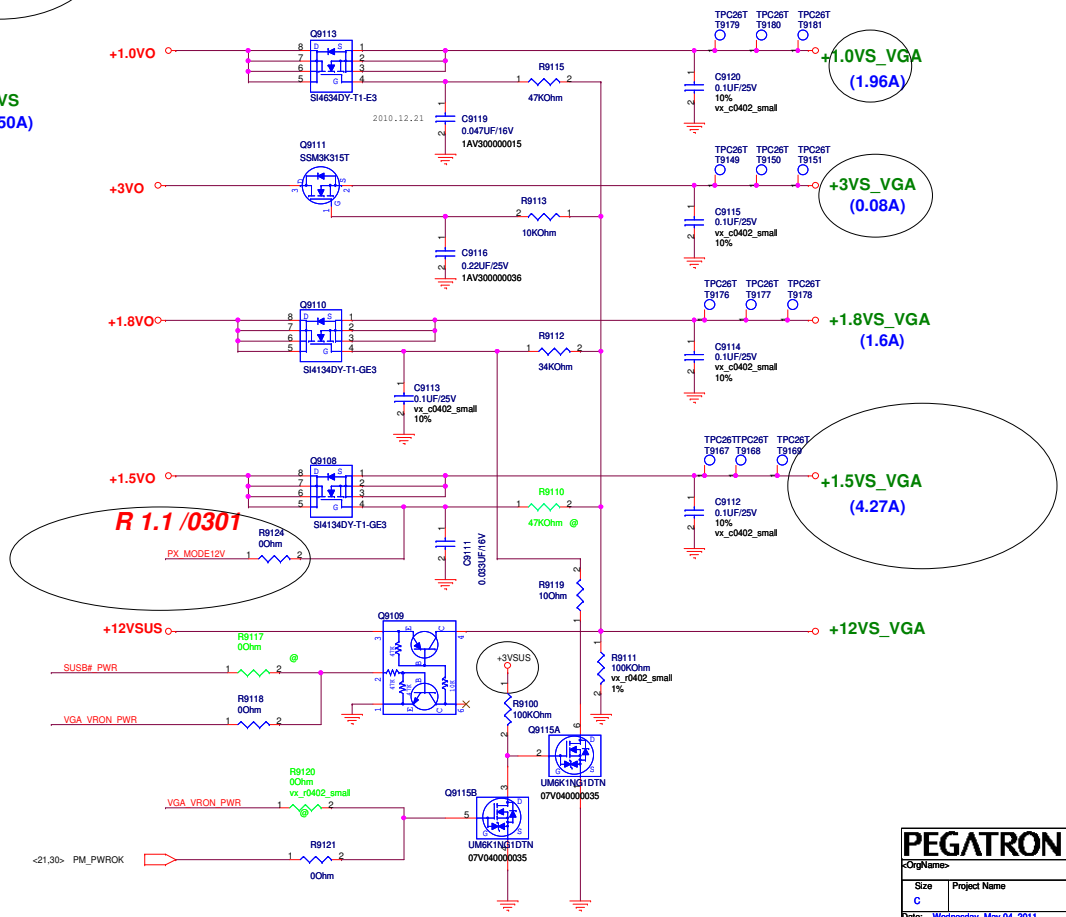




SUSC#_PWR POWER

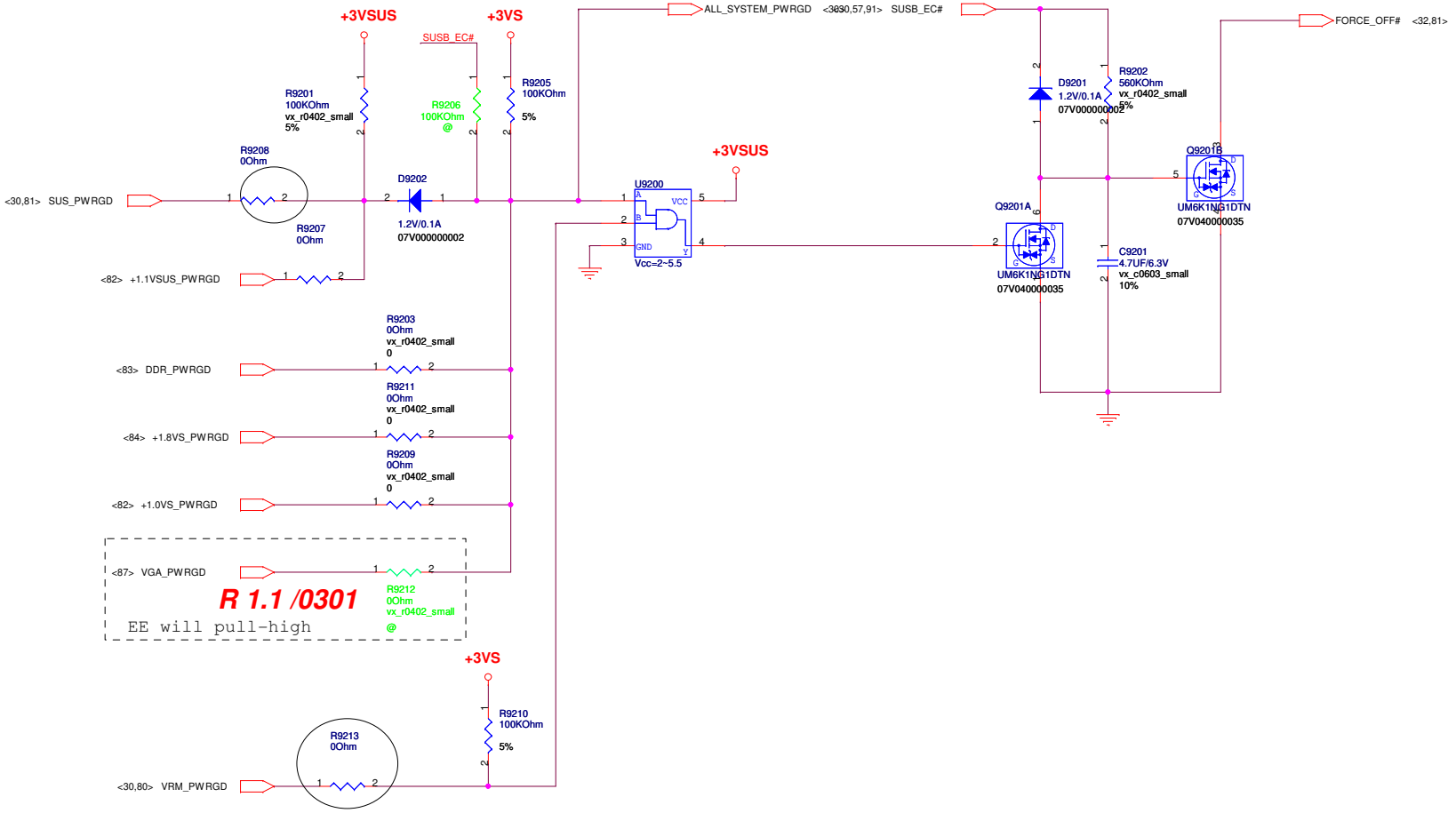


VGA_VRON_PWR_PWR POWER



PEGATRON	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Louis	
Size: C	Project Name	Rev: 1.0
Date: Wednesday, May 04, 2011	Sheet 91 of 99	

POWER GOOD DETECTER



PEGATRON	Title : POWER_PROTECT	
<OrgName>	Engineer: Louis	
Size: Custom	Project Name	Rev: 1.0
Date: Wednesday, May 04, 2011	Sheet 92 of 99	

AC_BAT_SYS — AC_BAT_SYS <45,66,80,81,82,83,87,88>

+3VA — +3VA <20,22,30,52,56,57,81>
+RTC_POWER — +RTC_POWER <81>
+5VA — +5VA <52,56,81,87,88>
+5VAO — +5VAO <81,84>

+5VO — +5VO <81,91>
+3VO — +3VO <81,91>
+3VSUS — +3VSUS <4,20,21,23,24,28,30,33,81,92>
+5VSUS — +5VSUS <51,52,56,66,81,82,83,84,87>

+12VSUS — +12VSUS <22,51,81,91>
+12V — +12V <91>
+12VS — +12VS <48,91>

+3V — +3V <30,40,44,45,53,55,57,91>
+3VS — +3VS <4,5,7,8,21,22,23,24,30,31,32,33,36,37,38,39,45,48,50,51,53,56,57,80,91,92>
+3VS_VGA — +3VS_VGA <57,70,71,75,78,91>
+5V — +5V <45,55,56,57,91>
+5VS — +5VS <30,31,36,38,46,48,50,51,56,57,80,91>
+1.1VO — +1.1VO <82,91>
+1.1VSUS — +1.1VSUS <23,82>
+1.1VS — +1.1VS <23,57,91>
+1.8VO — +1.8VO <84,91>
+1.8VS — +1.8VS <4,5,57,80,84>
+1.8VS_VGA — +1.8VS_VGA <57,71,74,75,78,91>
+0.75VS — +0.75VS <7,8,57,83>
+0.75VO — +0.75VO <83>
+1.5VO — +1.5VO <83,91>
+1.5VS — +1.5VS <53,57,91>
+1.5V — +1.5V <3,5,7,8,45,55,57,83>
+1.5VS_VGA — +1.5VS_VGA <57,72,73,75,91>
+1.0VO — +1.0VO <82,91>
+1.0VS — +1.0VS <3,5,57,82>
+1.0VS_VGA — +1.0VS_VGA <57,70,71,74,75,91>

+VCORE — +VCORE <5,80>
+VCORE_O — +VCORE_O <80>

+VDDCR_NB — +VDDCR_NB <5,80>
+VDDCR_NB_O — +VDDCR_NB_O <80>

+VDDC_VGA — +VDDC_VGA <75,87>
+VDDC_VGA_O — +VDDC_VGA_O <87>

BAT — BAT <88>
BAT_CON — BAT_CON <57,88>

FOR POWER TEST

+3VA

JP9300 — SGL_JUMP @ — CPU_VRON_PWR <80>
JP9301 — SGL_JUMP @ — SUSB#_PWR <82,83,84,87,91>
JP9302 — SGL_JUMP @ — SUSC#_PWR <83,91>
JP9303 — SGL_JUMP @ — VSUS_ON <22,30,81,82>
JP9304 — SGL_JUMP @ — VGA_VRON_PWR <87,91>

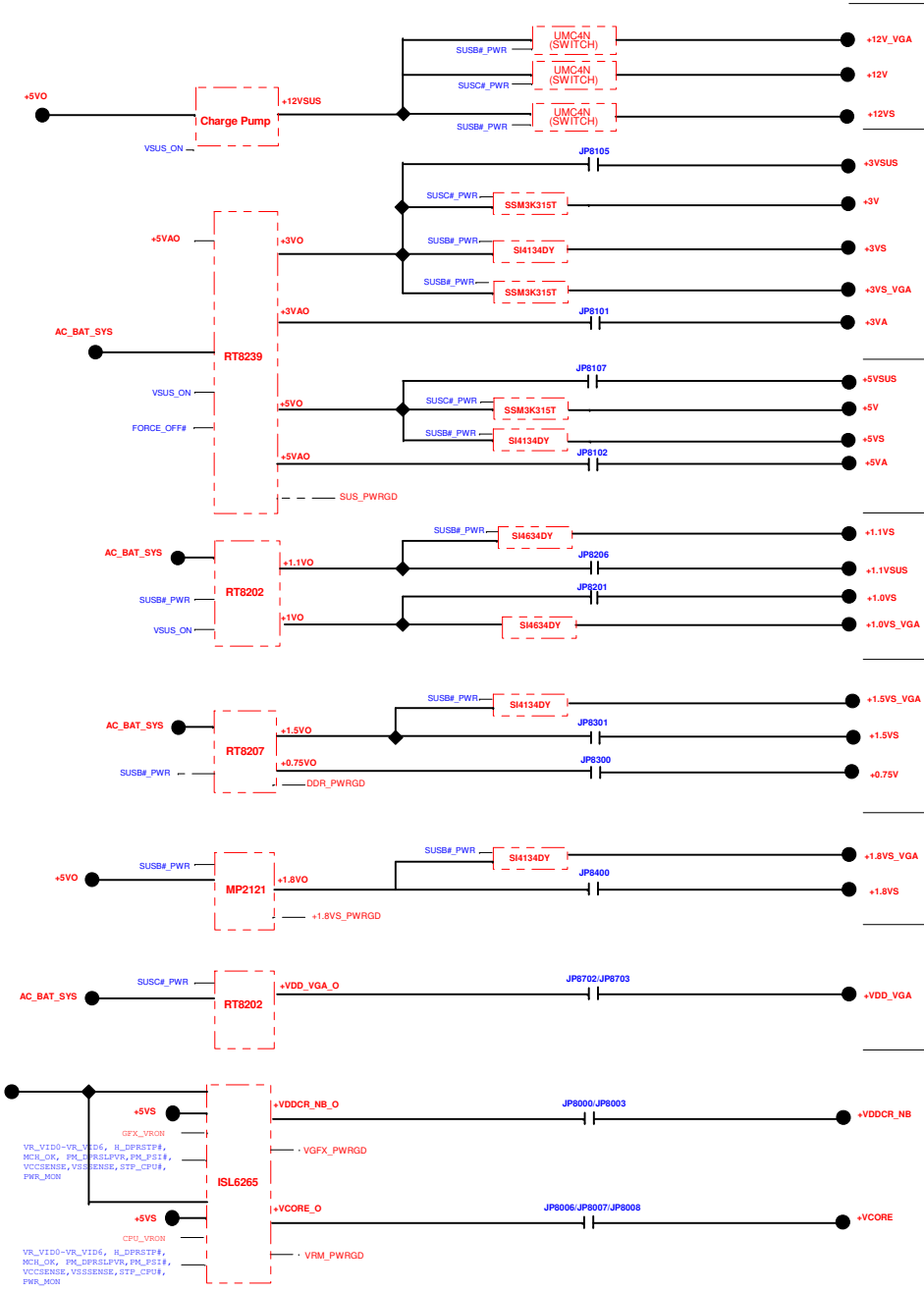
<Variant Name>

PEGATRON Title :POWER_SIGNAL

Engineer: Louis

Size	Project Name	Rev
B		1.0

Date: Wednesday, May 04, 2011 Sheet 93 of 99



	SPEC rating	Design rating
+12V_VGA		
+12V		
+12VS		
+3VSUS	(1.37A)	(1.096A)
+3V	(1.485A)	(1.188A)
+3VS	(2.651A)	(2.121A)
+3VS_VGA	(0.19A)	(0.152A)
+3VA	(0.23A)	(0.184A)
+5VSUS	(3.57A)	(2.856A)
+5V	(0.04A)	(0.032)
+5VS	(4.251A)	(3.401A)
+5VA		
+1.1VS	(3.832A)	(3.066A)
+1.1VSUS	(0.39A)	(0.312A)
+1.0VS	(5.7A)	(3.99A)
+1.0VS_VGA	(2.8A)	(1.96A)
+1.5VS_VGA	(5.2A)	(3.64A)
+1.5VS	(0.8A)	(0.56A)
+0.75V	(1.5A)	(1.2A)
+1.8VS_VGA	(2A)	(1.6A)
+1.8VS	(2.3A)	(1.84A)
+VDD_VGA	(8.5A)	(5.95A)
+VDDCR_NB	(10A)	(7A)
+VCORE	(11A)	(7.7A)

R20

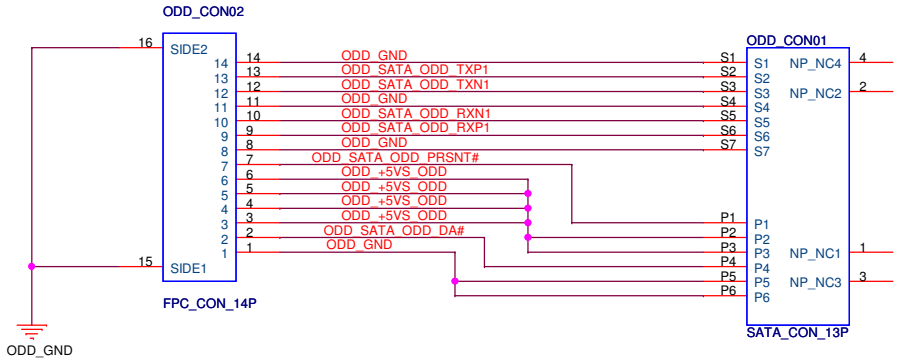
Item	Date	Description
1	0328-11	P.72 Add R7210~R7215, C7201, C7202 for VRAM Channel A reseved.
		P.5 Change C0508=>0805, L0501=>1K 0603 for CRT ripple noise.
		P.39 Add R3909, R3910, R3914, R3915 for POP issue
		P.50 Add R5010, C5020, C5021, Q5001, U5005 for Thermal Palm rest.
		P.04 Add SP0410, SP0411 for Thermal Palm rest.
		P.32 Add R3210 for Thermal Palm rest.
7	0330-11	P.98 Copy TP BTN Board from AIH24
8		P.66 Add 2nd USB power switch (U6605) for Audio board USB port voltage drop
9		P.50 Un-mount R5010, C5020, C5021, Q5001, U5005
10	0331-11	P.22 Add Test Pad T2201, T2202 for U2001.W5 and AE29 ICT function.
11		P38. Update CON3801, CON3802=>1217-00P1000
12		P66. Update CON6602=>1218-01BJ000
13		P99. Update IOCON5=>1218-01BJ000
14		P31. CON3102, CON3103=>1218-00C7000
15	0404-11	P65. Change H6539, H6541, H6542, H6545, H6633 to NPTH
16		P66. Change CON6603, CON6605 to 4 pin. Del C6605, C6608. Un-mount R6609
17		P97. Change PWR_U01 to 4 pin, delete PWR_R2, PWR_LED2
18	0406-11	P65. Modify H6541, H6542, H6545 GND
19		P33. Add L3303 for AVDDL EMI issue
20		P34. Add U3405 for EMI Home issue
21	0407-11	P66. Add CON6608
22		P99. Add IOCON6
23		P34. Un-mount R3408, R3409
24		P72. Un-mount C7201, C7202
25	0410-11	P39. R3905, R3906=> 51 ohm
26		P33. Mount R3317=> 10K
27		P46. Change L4601~L4603=> 56nH (Not yet)
28		P66. Change U6601=>1.5A, Mount U6605
29	0411-11	P30. Change R3035 option as /SJV_ID
30		P21. Change R3042 option as /SJV_ID
31	0421-11	P66. Change U6601, U6605 => 2.5A
32		P50. Change R5001 => 39K ohm for Thermal
33		P56. Change R5603,R5621 => 100 ohm,390 ohm；LED5610,R5611=> 0713-1QJ000,0713-1QK000
34		P33. Change C3321,C3322 => 15PF
35		P33. Change L3303 => 0 ohm (0603)
36		P46. Change L4601, L4602, L4603 => 56nH for EMI
37		Update Power AAB7A_BRAZO_PWR_2R0_0411_DSC_A& AIC70 Sub board AIC70_R20_201104211100
38	0503-11	P66 unmount con6608
39	0504-11	P34 Mount R3408
40		P65 Un-mount H6535, H6536
41		P99 Un-mount IOCON6
42		Update Power AAB7A_BRAZO_PWR_2R0_0504_DSC_A
43	0505-11	P39 Un-mount R3910, Mount R3914=1M ohm

PEGATRON Title : History

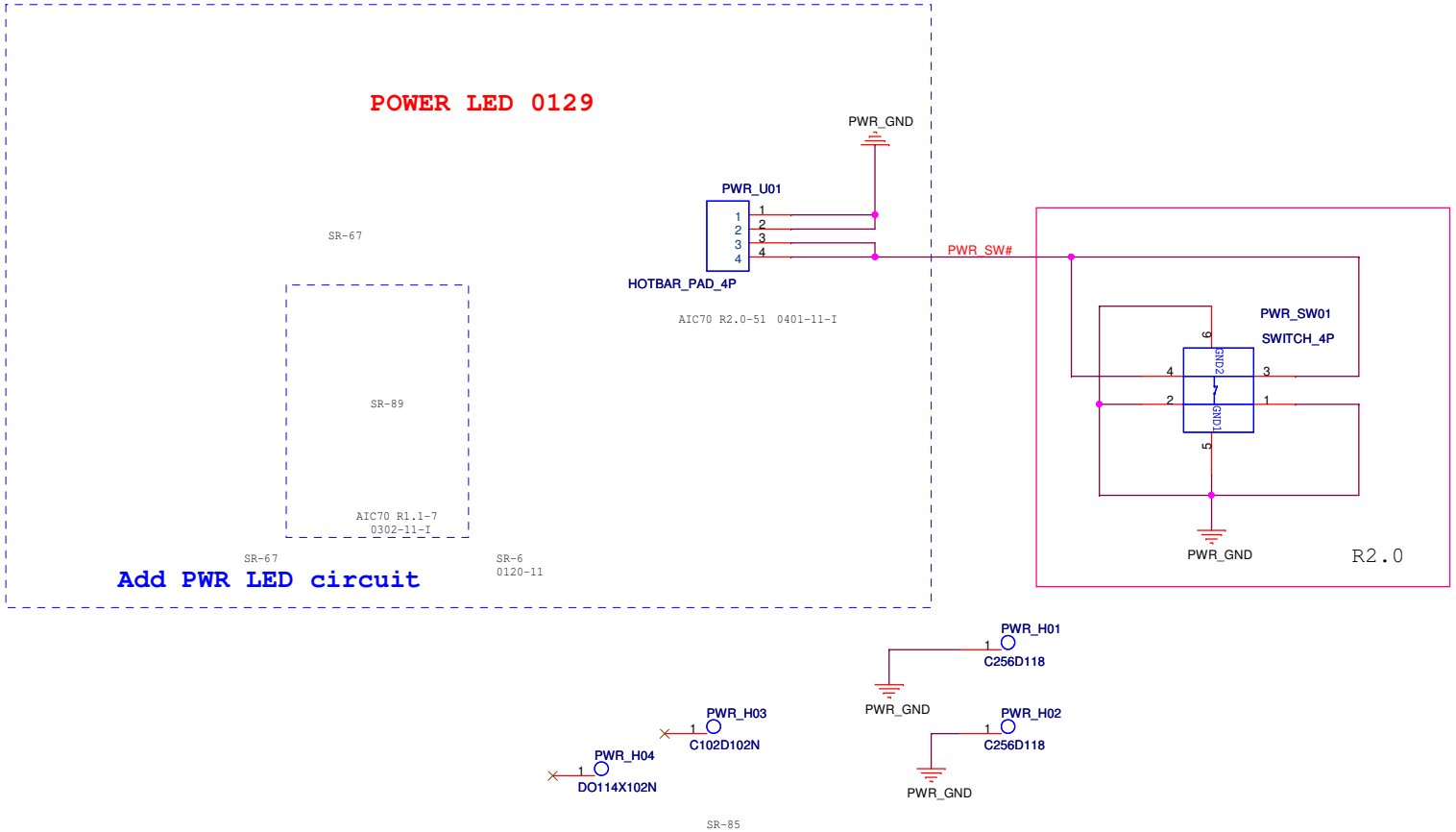
<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
B	AAB70	1.1

Date: Thursday, May 05, 2011 Sheet 95 of 99



PEGATRON	Title : ODD	
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang	
Size: B	Project Name: TOD ODD BOARD	Rev: 2.0
Date: Thursday, April 21, 2011	Sheet 96 of 77	



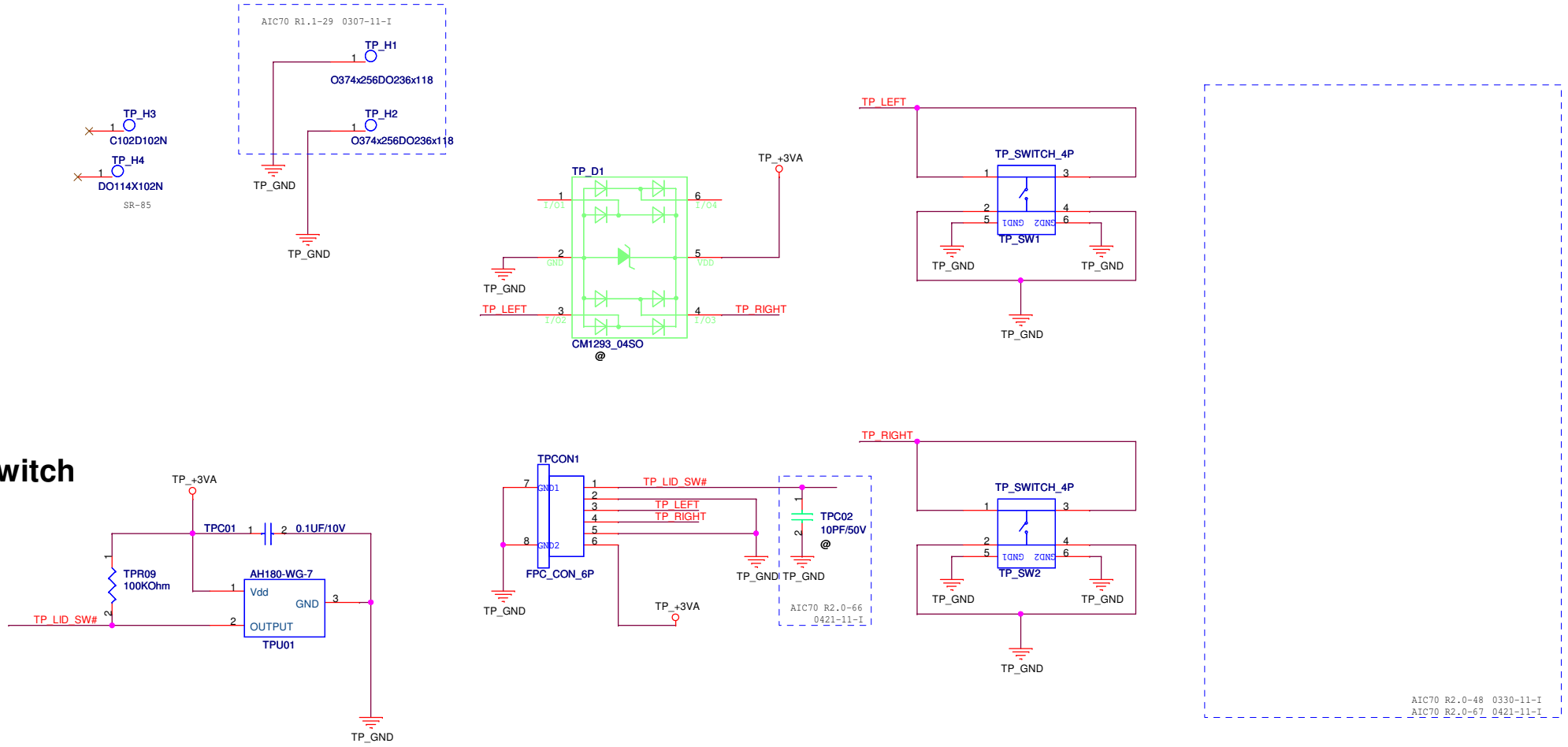
PEGATRON **Title :** PWR BTN

BU1-RD Div.1-HW RD Dept.1 **Engineer:** *Johnson Huang*

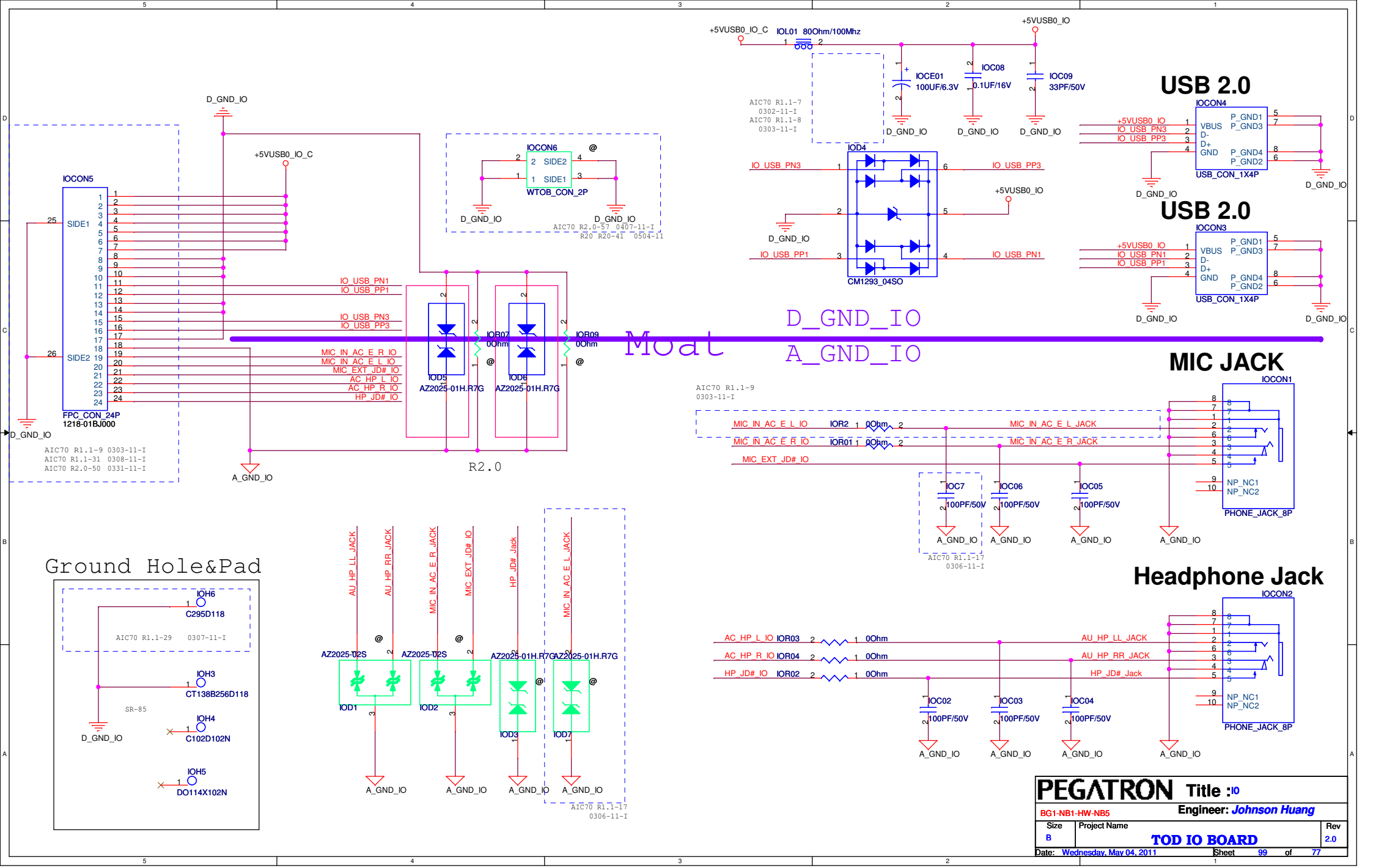
Size	Project Name	Rev
B	**TOD POWER SW**	2.0

Date: Thursday, April 21, 2011 Sheet 97 of 77

LID Switch



PEGATRON	Title : A03 TP	
<OrgName>	Engineer: Johnson Huang	
Size: B	Project Name: AIH70	Rev: 1.0
Date: Thursday, April 21, 2011	Sheet 98 of 99	


USB 2.0
USB 2.0
MIC JACK
Headphone Jack
Ground Hole&Pad
Moat
D_GND_IO
A_GND_IO
R2.0
IOCON5
FPC_CON_24P
1218-01BJ000
IOCON6
WTOB_CON_2P
IOD4
CM1293_04SO
IOD5
IOD6
AZ2025-01H.R7G
IOR07
IOR09
0Ohm
IOL01 80Ohm/100Mhz
IOCE01
100UF/6.3V
IOC08
0.1UF/16V
IOC09
33PF/50V
IOCON4
IOCON3
USB_CON_1X4P
IOCON1
IOCON2
PHONE_JACK_8P
IOR2
IOR01
IOR03
IOR04
IOR02
IOC7
IOC06
IOC05
IOC02
IOC03
IOC04
100PF/50V
IOD1
IOD2
IOD3
IOD7
AZ2025-02S
IOH6
C295D118
IOH3
CT138B256D118
IOH4
C102D102N
IOH5
DO114X102N
SR-85
PEGATRON
Title :IO
BG1-NB1-HW-NB5
Engineer: Johnson Huang
Size B
Project Name TOD IO BOARD
Rev 2.0
Date: Wednesday, May 04, 2011
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