

## FDS6612A

### Single N-Channel, Logic Level, PowerTrench™ MOSFET

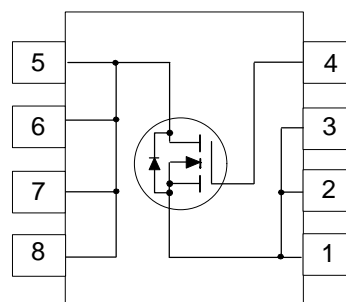
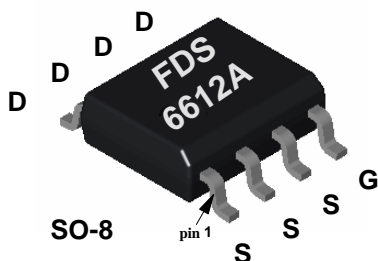
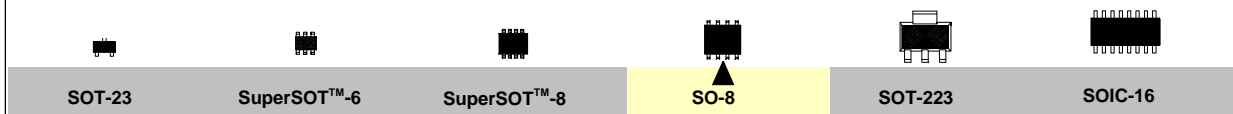
#### General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

#### Features

- 8.4 A, 30 V.  $R_{DS(ON)} = 0.022 \Omega @ V_{GS} = 10 \text{ V}$ ,  
 $R_{DS(ON)} = 0.030 \Omega @ V_{GS} = 4.5 \text{ V}$ .
- Fast switching speed.
- Low gate charge.
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.



#### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDS6612A	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	8.4	A
	- Pulsed	40	
$P_D$	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

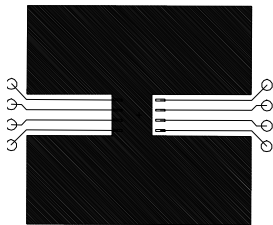
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

## Electrical Characteristics (T<sub>A</sub> = 25 °C unless otherwise noted)

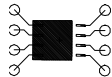
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25 °C		26		mV / °C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μA
		T <sub>J</sub> = 55°C			10	μA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
<b>ON CHARACTERISTICS (Note 2)</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.6	3	V
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Temp. Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25 °C		-4.3		mV / °C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8.4 A		0.019	0.022	Ω
		T <sub>J</sub> = 125°C		0.027	0.037	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.2 A		0.026	0.03	
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	20			A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 8.4 A		19		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		830		pF
C <sub>oss</sub>	Output Capacitance			185		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			80		pF
<b>SWITCHING CHARACTERISTICS (Note 2)</b>						
t <sub>D(on)</sub>	Turn - On Delay Time	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 A		6	12	ns
t <sub>r</sub>	Turn - On Rise Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		10	18	ns
t <sub>D(off)</sub>	Turn - Off Delay Time			18	29	ns
t <sub>f</sub>	Turn - Off Fall Time			5	12	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 8.4 A,		9	13	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 5 V		2.8		nC
Q <sub>gd</sub>	Gate-Drain Charge			3.1		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2.1	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.1 A (Note 2)		0.75	1.2	V

### Notes:

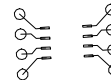
- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 50°C/W on a 1 in<sup>2</sup> pad of 2oz copper.



b. 105°C/W on a 0.04 in<sup>2</sup> pad of 2oz copper.



c. 125°C/W on a 0.006 in<sup>2</sup> pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

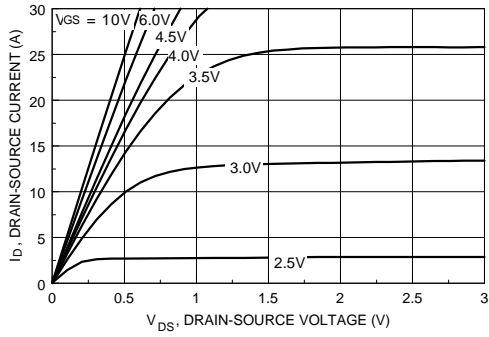


Figure 1. On-Region Characteristics.

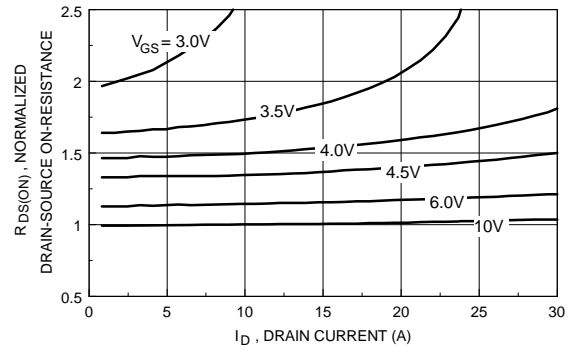


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

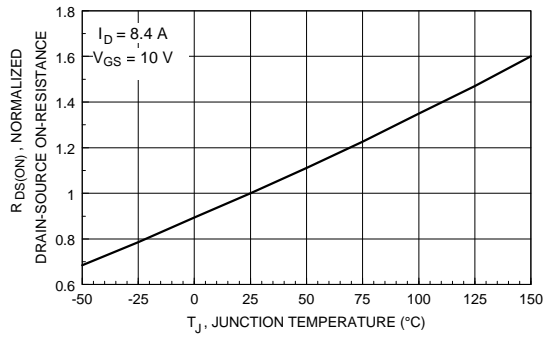


Figure 3. On-Resistance Variation with Temperature.

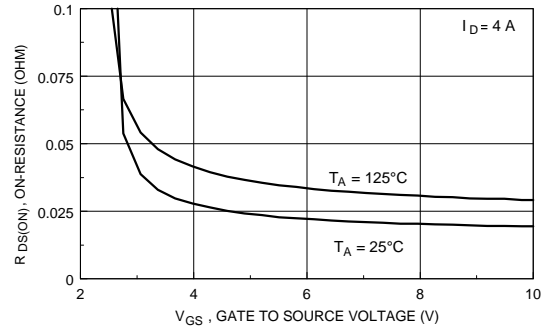


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

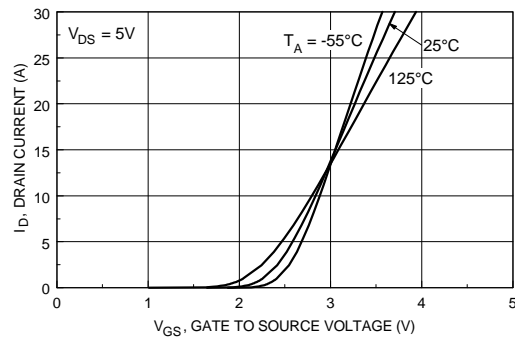


Figure 5. Transfer Characteristics.

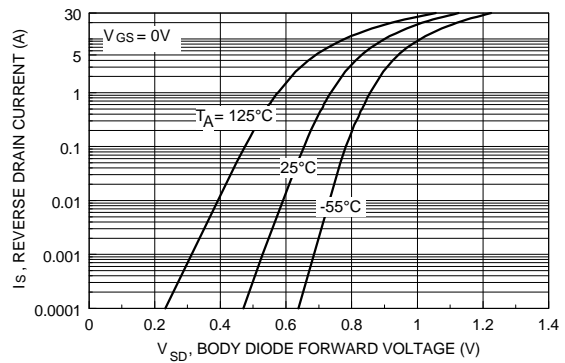


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical And Thermal Characteristics

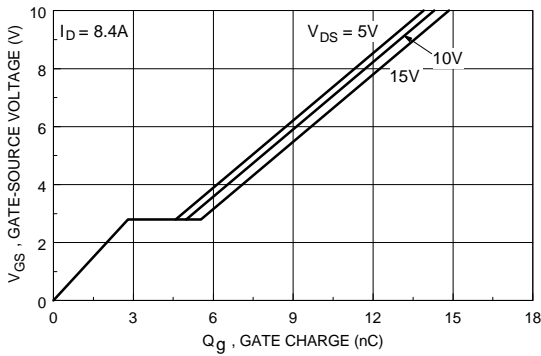


Figure 7. Gate Charge Characteristics.

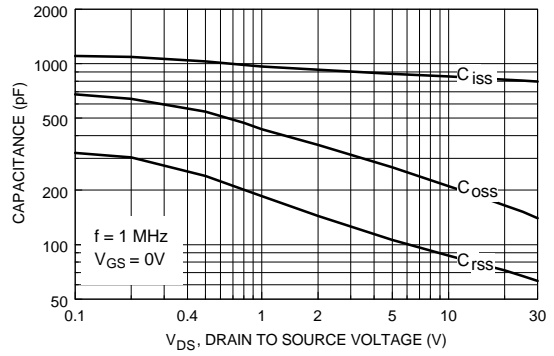


Figure 8. Capacitance Characteristics.

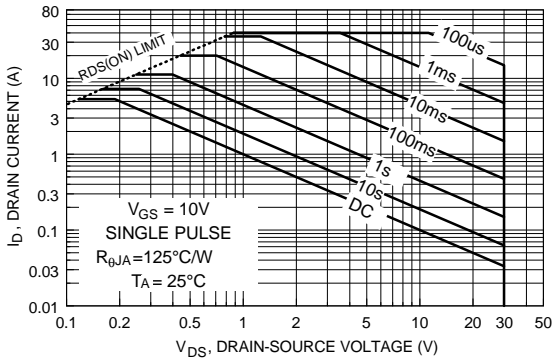


Figure 9. Maximum Safe Operating Area.

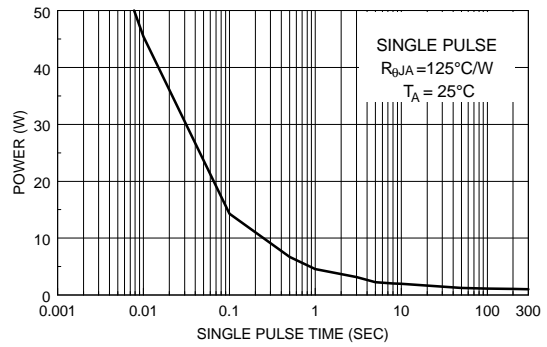


Figure 10. Single Pulse Maximum Power Dissipation.

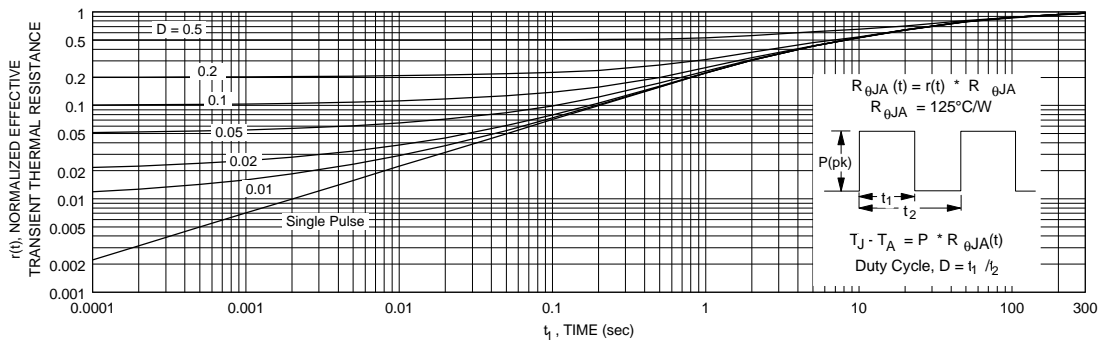


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	ISOPLANAR™	TinyLogic™
CoolFET™	MICROWIRE™	UHC™
CROSSVOLT™	POP™	VCX™
E <sup>2</sup> CMOS™	PowerTrench™	
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	
HiSeC™	SuperSOT™-8	

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.