R2600
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

l CPU Core
- RDC's proprietary RISC architecture
- Five-stage pipeline architecture
- Operation frequency: 100MHz
- Supports a 8K-byte uniform cache

l ROM/RAM/SDRAM Controller and Addressing Space
- Supports 16-bit data bus width
- Flash ROM / SRAM control interface
- SDRAM control interface
- 16M addressing space
- 64K-byte I / O space

l Two Independent DMA Controllers
- Supports high-speed DMA transfers

l Interrupt Controller
- Provides 8 maskable external interrupt channels

l Counter/Timers
- Three independent programmable 16-bit timers
- One programmable watchdog timer which can generate NMI or reset.

l High Performance UART Ports
- Supports 2 high performance UARTs with send / receive 16-byte FIFOs
- Programmable baud rate generator

l IEEE 802.11b/g WLAN Support
- Security: 64 / 128 WEP, WPA, AES
- Advanced power saving algorithm for dynamic network traffic environment
- The data rates are programmable from 50 to 460.8K baud (max. to 1Mbps)
- The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd or no parity, 5~8 data bits

l RDC Debug Tool Support
- RDC debug tool with a JTAG-like interface

l General Programmable I/O
- 48 programmable I / O ports mixed with other functions
- 8 dedicated GPIOs for WLAN block
- Pins individually configurable to input or output mode

l Two 10/100M Fast Ethernet MAC Ports
- IEEE 802.3u MII interface
- IEEE 802.3x flow control in full-duplex mode
- Internal loop-back self-test circuit support
- Descriptor architecture for packet TX / RX

l PCI Control Interface Support
- Supports up to 3 PCI masters
- Speed up to 33MHz

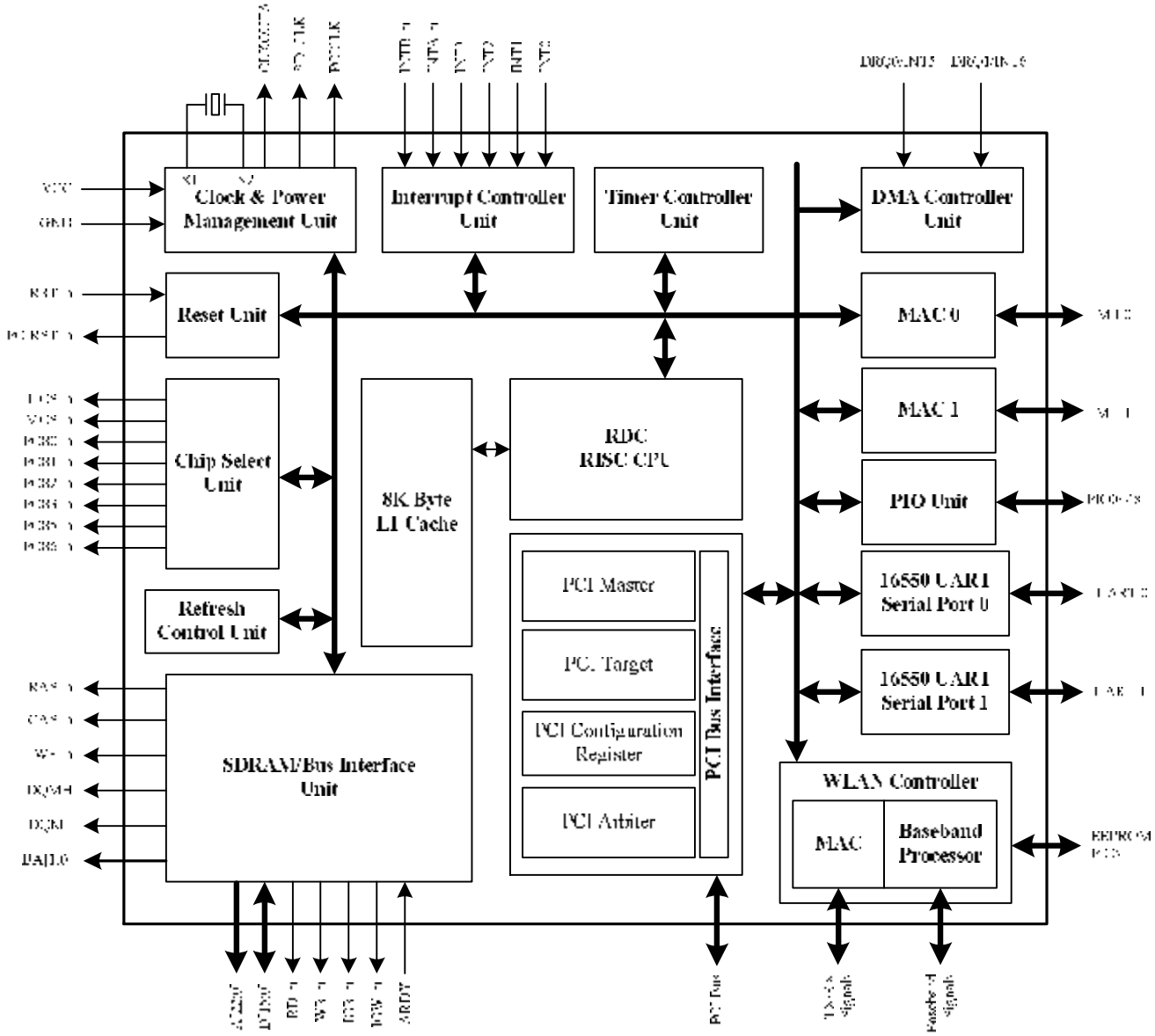
l Two Card Bus Interface Support

- On-chip A / D and D / A Converters for I / Q data, TSSI and AGCs.
- Supports 6, 9, 12, 18, 24, 36, 48, 54 Mbps for OFDM; 5.5, 11Mbps for CCK; and 1,2 Mbps for barker

modulation.
- Supports short preamble and antenna diversity
- Proprietary robust demodulator with patent protection
- Mitigates multipath delay spread up to 100ns at 54Mbps
- 2 configurable LEDs to release CPU from LED routine loading

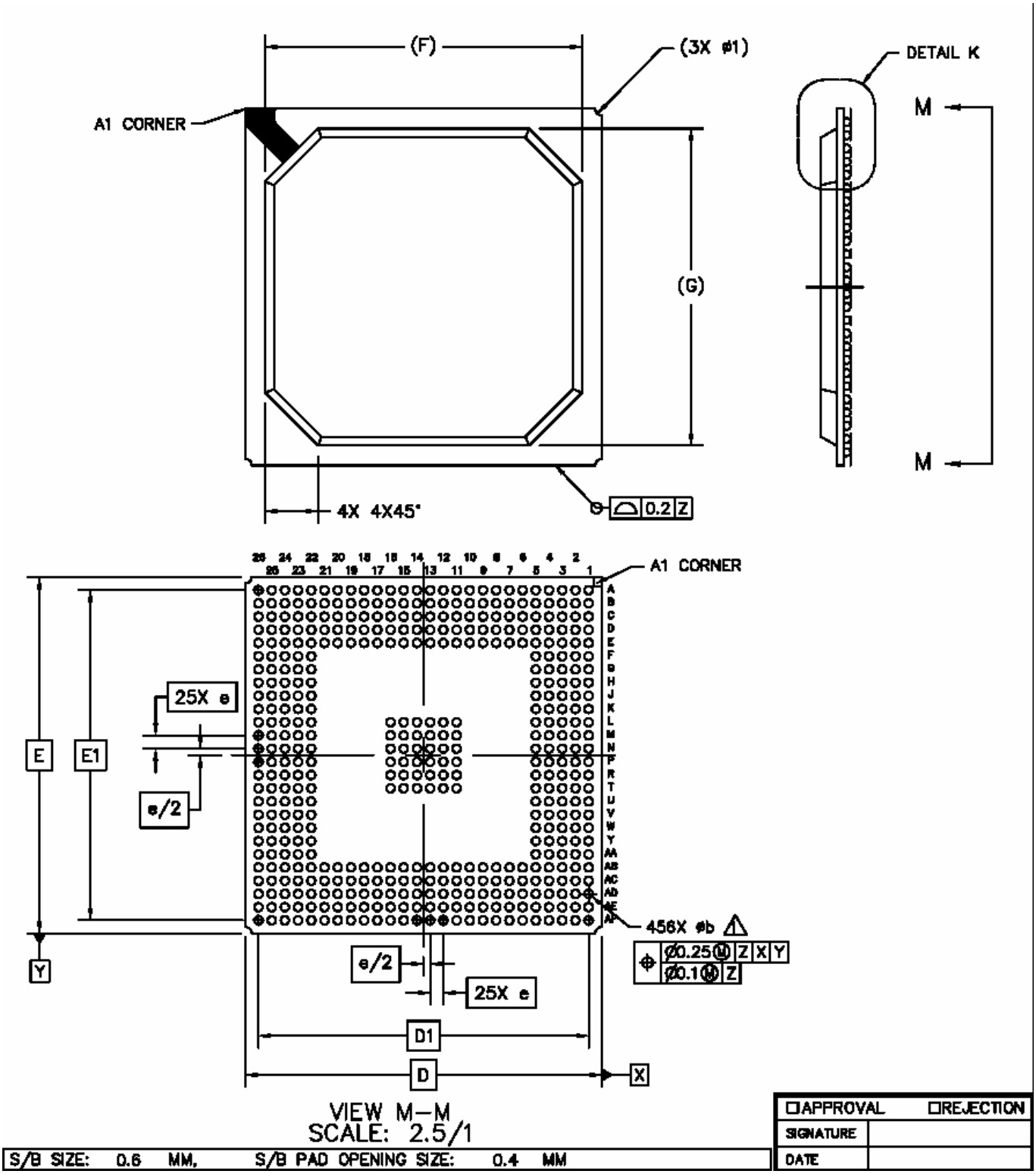
l A Lead-free Product

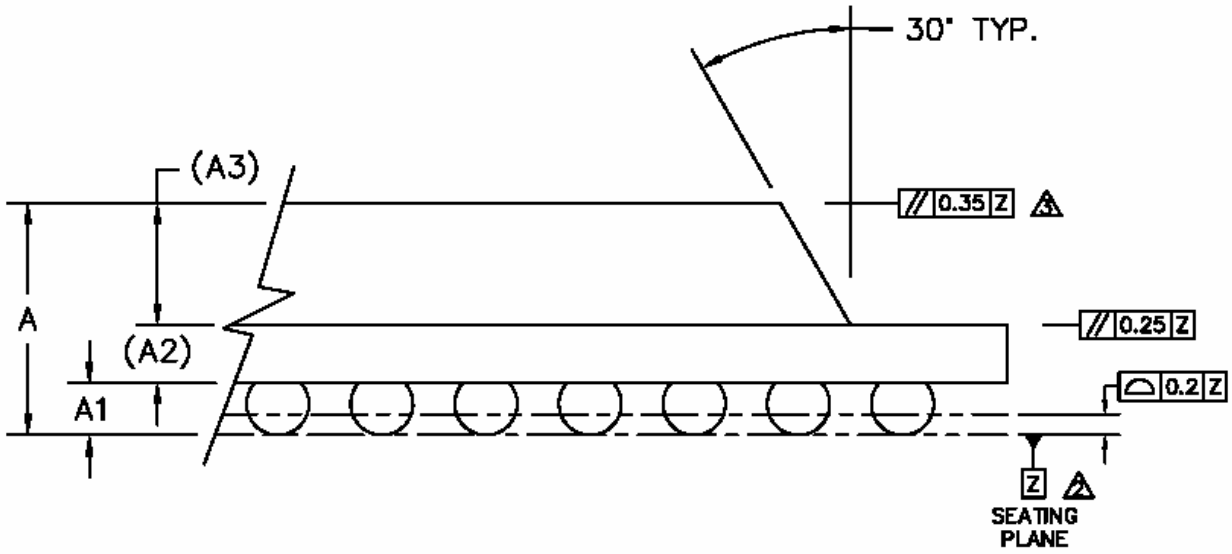
2. Block Diagram



3. Package Information

BGA Package Drawing: PBGA 456 Balls





DETAIL K
SCALE: 15/1
(ROTATE 90°)

DIM	MIN.	NOR.	MAX.
A	---		2.36
A1	0.4		0.6
A2		0.56 REF	
A3		1.17 REF	
b	0.5		0.7
D		27 BSC	
E		27 BSC	
e		1 BSC	
D1		25 BSC	
E1		25 BSC	
G		24 REF	
F		24 REF	

NOTES

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	JEDEC–MS–034

TITLE:	COMPANY	ASECL
PBGA 456 BALLS 27X27X2.36 PKG 1 PITCH POD	SHEET	2 OF 3