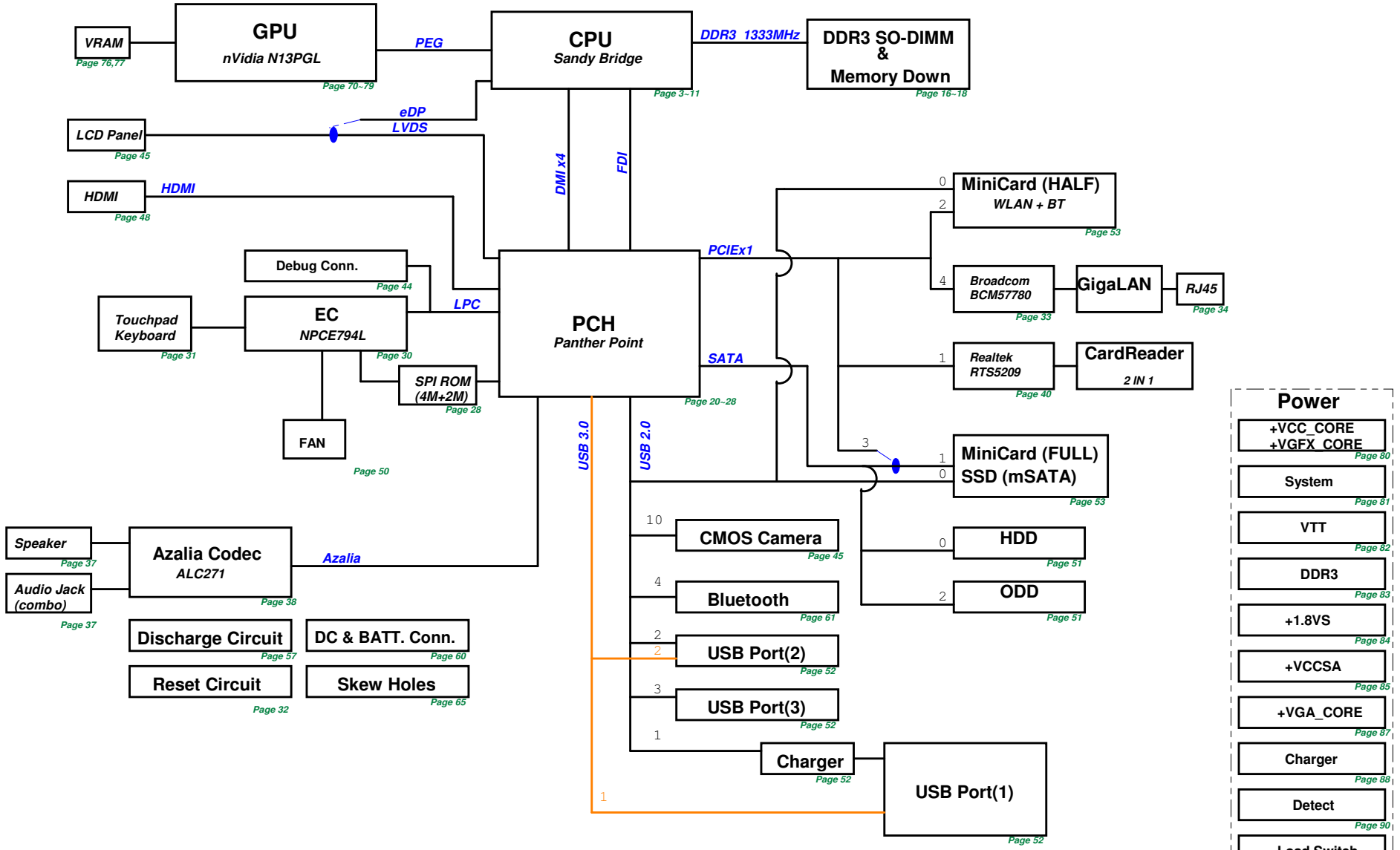
JM50 Ultrabook Block Diagram Rev 1.0



PEGATRON Title : Block Diagram

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 1 of 93

PCH_CPT GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
GPIO 37				
GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
GPIO 46				
GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

EC NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
GPG0		
GPG1		
GPG2		
GPG6		
GPH0		
GPH1		
GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

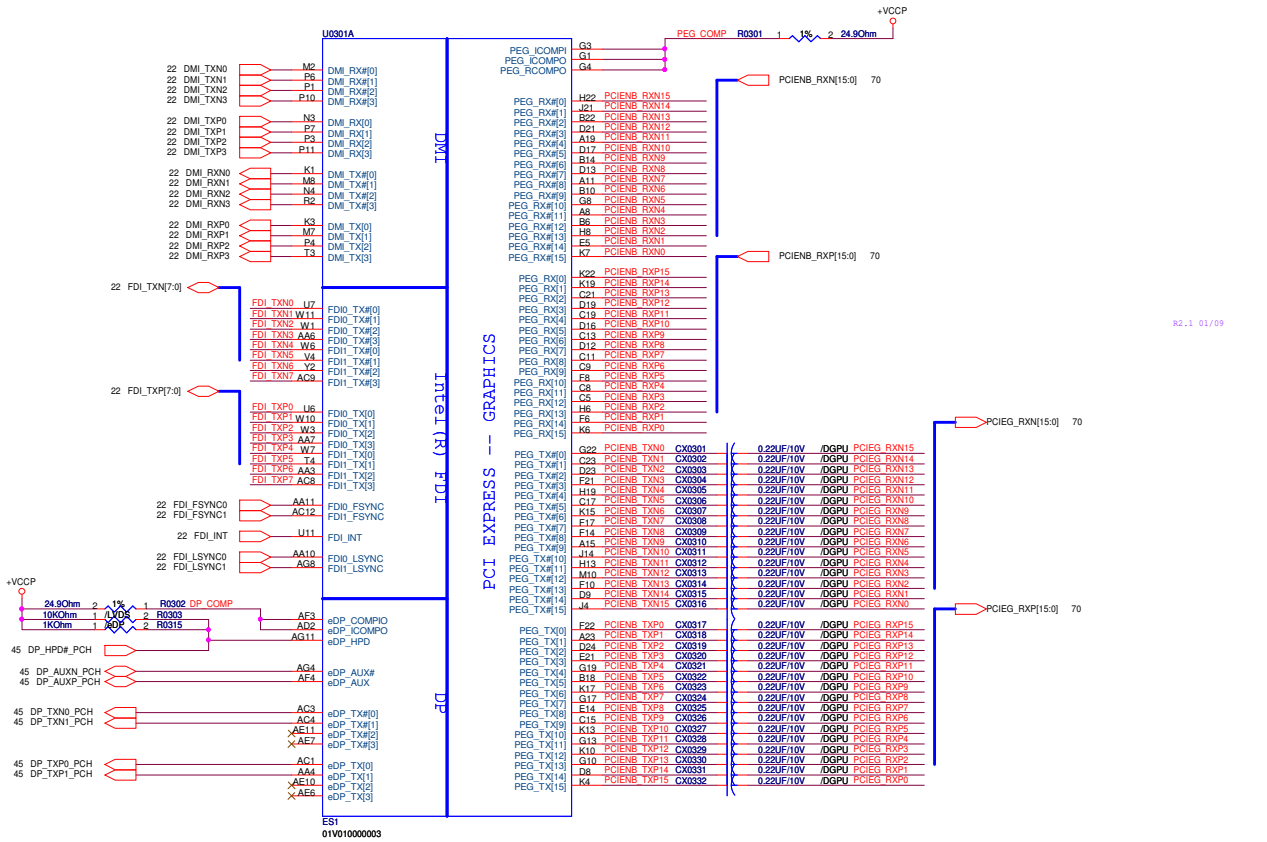
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

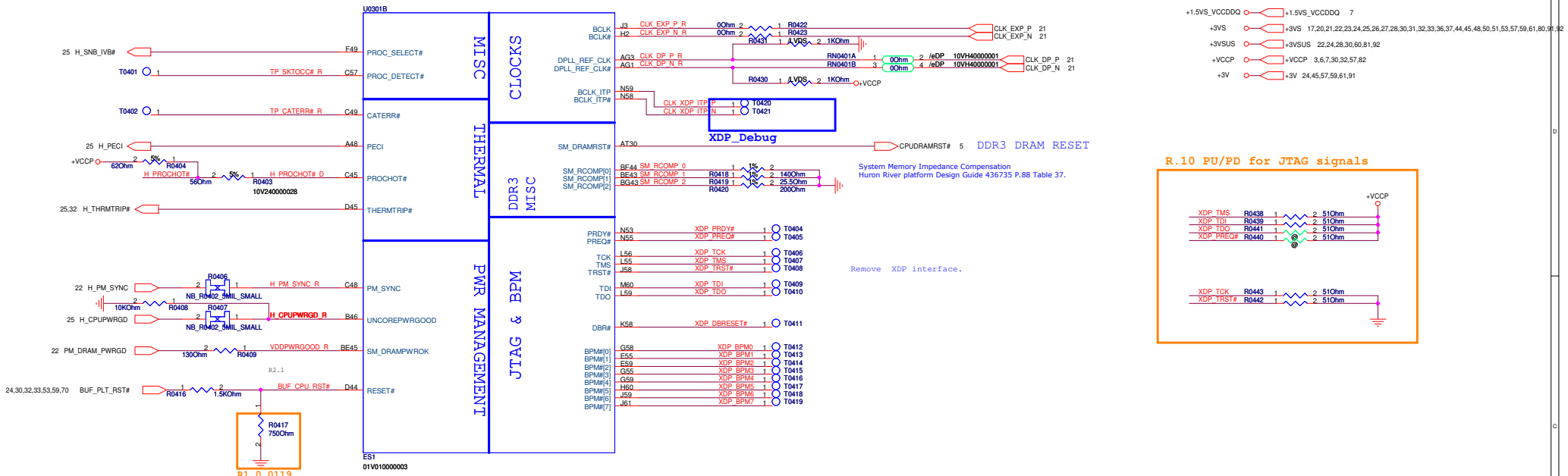
Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 2 of 93



R2.1 01/09

PEGATRON	Title : CPU(1)_DMI,DP,PEG,FDI	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 3 of 93	

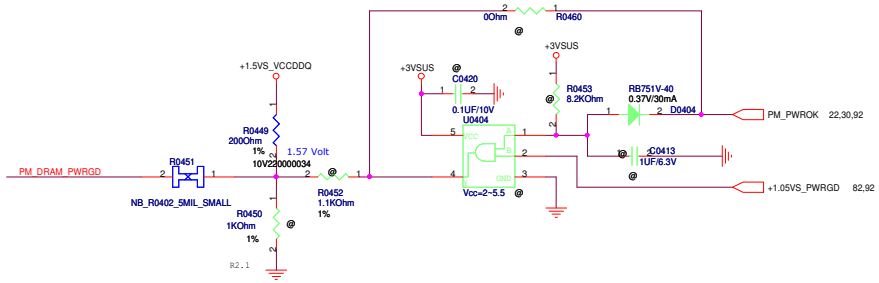


R1.0 0119
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

R.10 PU/PD for JTAG signals

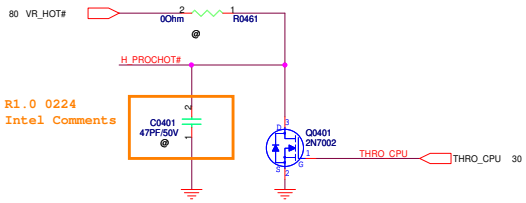
PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

Different from EVEREST



R1.1
add S3 power reduction

If support S3 power reduction with power good.
1. Mount U0404, D0404, C0413, C0420, R0450, R0452, R0453,
   Unmount R0460
2. Change R0449 to 1kohm from 200ohm, change R0409 to 0ohm from 130ohm - Design Guide 1.0 page 106



R1.0 0224
Intel Comments

PEGATRON Title : CPU(2)_CLK,MISC,JTAG

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 4 of 93

+1.5V +1.5V 16,17,18,57,60,83

U0301C

DDR SYSTEM MEMORY A

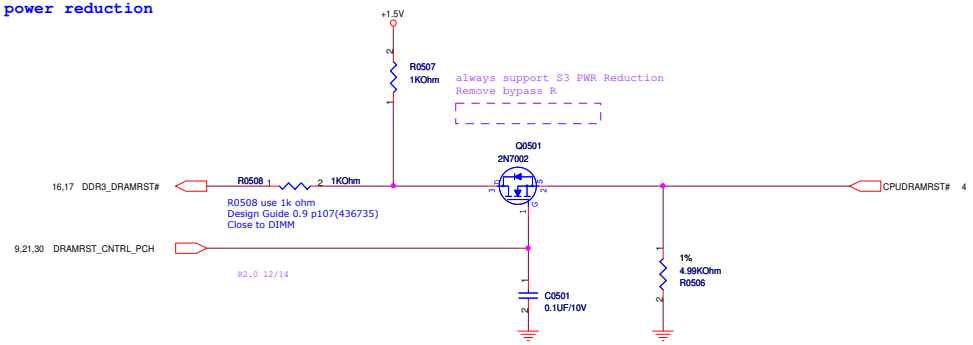
ES1
01V010000003

U0301D

DDR SYSTEM MEMORY B

ES1
01V010000003

R1.0 S3 circuit: DRAM_RST# to memory should be high during S3
R1.1 add S3 power reduction

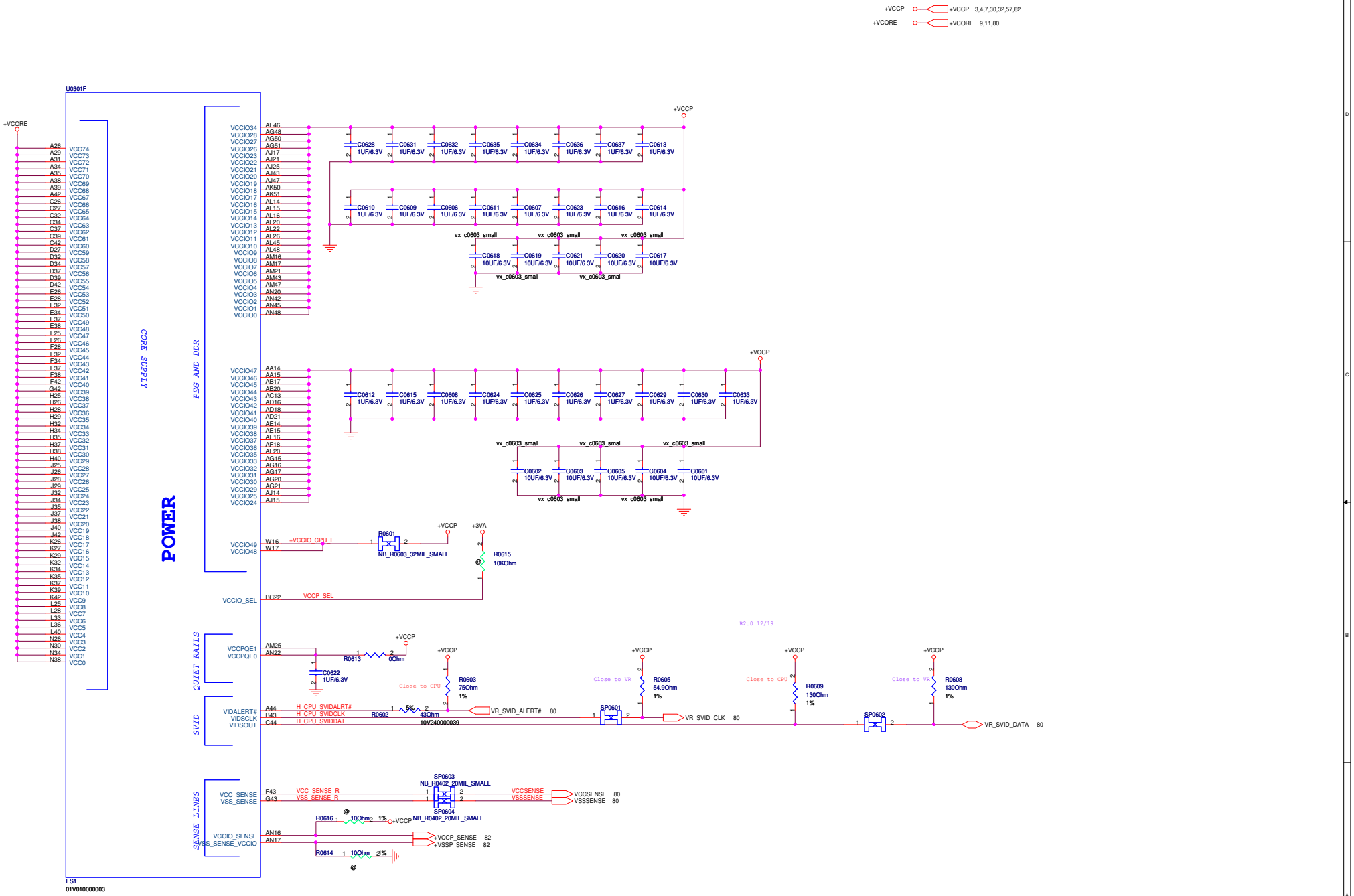


PEGATRON Title : CPU(3)_DDR3

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 5 of 93



PEGATRON	Title : CPU(4)_PWR		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 6 of 93		

Decoupling guide from Intel PDDG R0.8
+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 8pcs(power request)

+VCCP +VCCP 3,4,6,30,32,57,82
+1.5V +1.5V 5,16,17,18,57,60,83
+VCCSA +VCCSA 85
+1.8VS +1.8VS 25,26,57,80,84
+VGFX_CORE +VGFX_CORE 9,80
+1.5VS +1.5VS 26,53,57,91
+V_SM_VREF +V_SM_VREF 83

Graphics core voltage
Voltage range: 0 ~ 1.52V

+VGFX_CORE
C0725 1UF/6.3V C0727 1UF/6.3V C0731 1UF/6.3V C0726 1UF/6.3V C0732 1UF/6.3V C0729 1UF/6.3V C0730 1UF/6.3V C0728 1UF/6.3V
C0717 1UF/6.3V C0719 1UF/6.3V C0722 1UF/6.3V
vx_c0603_small: C0790 10UF/6.3V C0791 10UF/6.3V C0788 10UF/6.3V C0789 10UF/6.3V C0787 10UF/6.3V C0786 10UF/6.3V
C0738 22UF/6.3V C0739 22UF/6.3V C0740 22UF/6.3V C0741 22UF/6.3V C0742 22UF/6.3V C0743 22UF/6.3V C0744 22UF/6.3V C0745 22UF/6.3V

U0301G

AA46 VAXG21 AB47 VAXG20 AB50 VAXG19 AB51 VAXG18 AB52 VAXG17 AB53 VAXG16 AB55 VAXG15 AB56 VAXG14 AB58 VAXG13 AB59 VAXG12 AC61 VAXG11 AD47 VAXG10 AD48 VAXG9 AD50 VAXG8 AD51 VAXG7 AD52 VAXG6 AD53 VAXG5 AD55 VAXG4 AD56 VAXG3 AD58 VAXG2 AD59 VAXG1 AE46 VAXG0
N45 VAXG55 P47 VAXG54 P48 VAXG53 P50 VAXG52 P51 VAXG51 P52 VAXG50 P53 VAXG49 P55 VAXG48 P56 VAXG47 P61 VAXG46 T48 VAXG45 T58 VAXG44 T59 VAXG43 T61 VAXG42 U46 VAXG41 V47 VAXG40 V48 VAXG39 V50 VAXG38 V51 VAXG37 V52 VAXG36 V53 VAXG35 V55 VAXG34 V56 VAXG33 V58 VAXG32 V59 VAXG31 W50 VAXG30 W51 VAXG29 W52 VAXG28 W53 VAXG27 W55 VAXG26 W56 VAXG25 W61 VAXG24 Y48 VAXG23 Y61 VAXG22

GRAPHICS

POWER

DDR3 - 1.5V RAILS

SM_VREF AY43 +V_SM_VREF

DDR3 Reference Voltage

+1.5VS_VCCDDQ
R1.1
add S3 power reduction

+V_SM_REF 10mil
+V_SM_VREF
R0703 1KOhm
R0710 1KOhm
C0794 0.1UF/10V

VDDQ25 AJ28 VDDQ24 AJ33 VDDQ23 AJ36 VDDQ22 AJ40 VDDQ21 AL30 VDDQ20 AL34 VDDQ19 AL38 VDDQ18 AL42 VDDQ17 AM33 VDDQ16 AM36 VDDQ15 AM40 VDDQ14 AN30 VDDQ13 AN34 VDDQ12 AN38 VDDQ11 AR26 VDDQ10 AR28 VDDQ9 AR30 VDDQ8 AR32 VDDQ7 AR34 VDDQ6 AR36 VDDQ5 AR40 VDDQ4 AV41 VDDQ3 AW26 VDDQ2 BA40 VDDQ1 BB28 VDDQ0 BG33

MAX:5A

Processor I/O supply voltage for DDR3 (DC + AC specification)

+1.5VS_VCCDDQ JP0701 +1.5VS
@ 3MM_OPEN_5MIL
ICCMAX_VDDQ 5A

C0704 1UF/6.3V C0709 1UF/6.3V C0705 1UF/6.3V C0706 1UF/6.3V C0707 1UF/6.3V C0708 1UF/6.3V C0713 1UF/6.3V C0710 1UF/6.3V C0712 1UF/6.3V C0711 1UF/6.3V
vx_c0603_small: C0775 10UF/6.3V C0774 10UF/6.3V C0772 10UF/6.3V C0769 10UF/6.3V C0767 10UF/6.3V C0765 10UF/6.3V C0770 10UF/6.3V C0768 10UF/6.3V
CE0702 330UF/2V

R1.1
add S3 power reduction

Chief River

Decoupling guide from Intel (EE)
+1.5VS_VCCDDQ
1uF * 10pcs
10uF * 8pcs
330uF * 1pcs

Filtered(BGA Only)

VCCDQ1 AM28 VCCDQ0 AN26
+1.5VS_VCCDDQ R0707 0Ohm C0714 1UF/6.3V

QUIET RAILS

SP0701 NB_R0402_20MIL_SMALL
80 VCCGT_SENSE
80 VSSGT_SENSE
SP0702 NB_R0402_20MIL_SMALL
F45 VAXG_SENSE G45 VSSAXG_SENSE

SENSE LINES

PLL supply voltage
(DC + AC specification)

+1.8VS
MAX:1.2A
TDC: 1.2A
BB3 VCCPLL2 BC1 VCCPLL1 BC4 VCCPLL0
CE0701 330UF/2V C0761 1UF/6.3V C0764 1UF/6.3V

1.8V RAIL

+VCCSA
MAX:10A
TDC: 6A
vx_c0603_small: C0783 10UF/6.3V C0781 10UF/6.3V C0792 10UF/6.3V C0777 10UF/6.3V C0793 10UF/6.3V
C0735 1UF/6.3V C0736 1UF/6.3V C0733 1UF/6.3V C0734 1UF/6.3V C0737 1UF/6.3V
L17 VCCSA15 L21 VCCSA14 N16 VCCSA13 N20 VCCSA12 N22 VCCSA11 P17 VCCSA10 P20 VCCSA9 R16 VCCSA8 R18 VCCSA7 R21 VCCSA6 U15 VCCSA5 V16 VCCSA4 V17 VCCSA3 V18 VCCSA2 V21 VCCSA1 W20 VCCSA0

SA RAIL

SENSE LINES

VDDQ_SENSE BC43 VSS_SENSE_VDDQ BA43 T0701 T0702

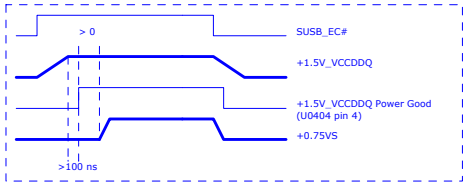
VCCSA_SENSE U10 R0704 0Ohm Close to CPU VCCSA_SENSE 85

VCCSA_VID[0] D48 VCCSA_VID[1] D49 VCCSA_SEL0 VCCSA_SEL1 VCCSA_SEL0 85 VCCSA_SEL1 85

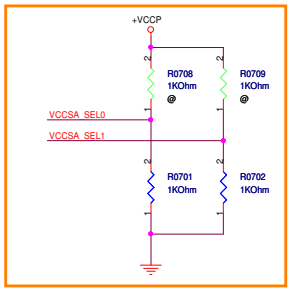
Chief River

R2.2, 03/05

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V



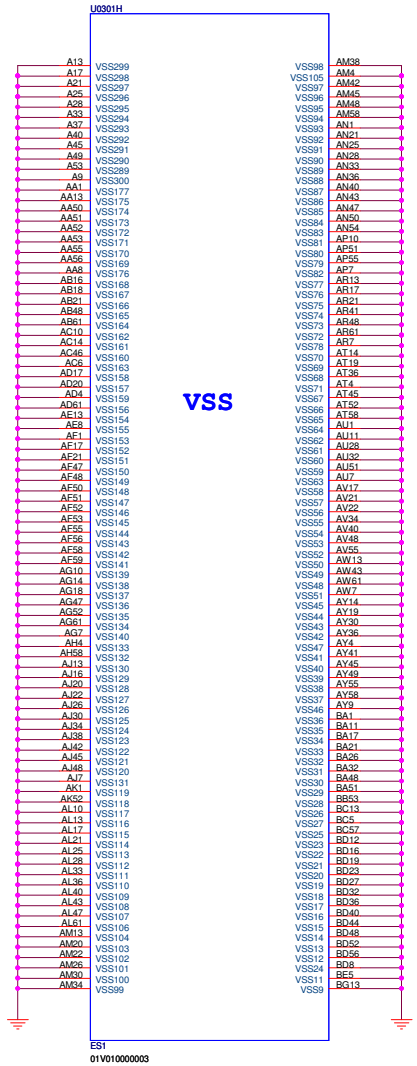
R1.0 0209
Intel Comments

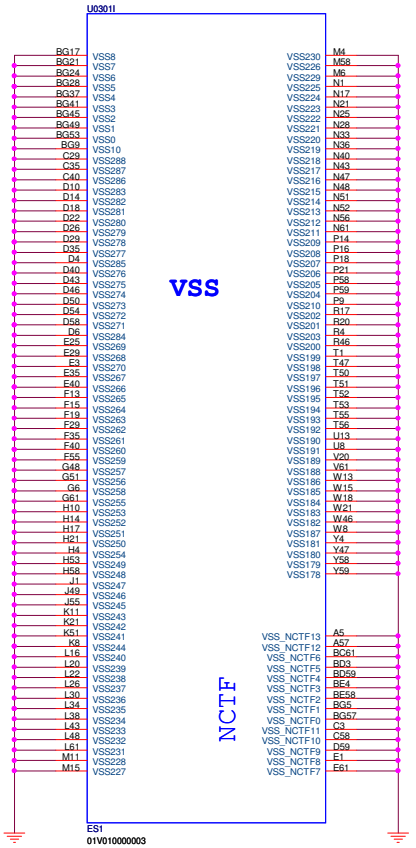


Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

ES1
01V010000003

PEGATRON	Title :	CPU(5)_GFX_PWR	
BG1-HW RD Div.2-NB RD Dept.5	Engineer:	Joyoung_Chianhg	
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 7 of 93		





PEGATRON	Title : CPU(6)_GND	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 8 of 93	

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection

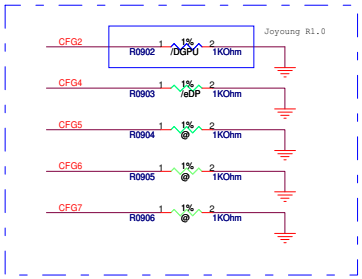
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

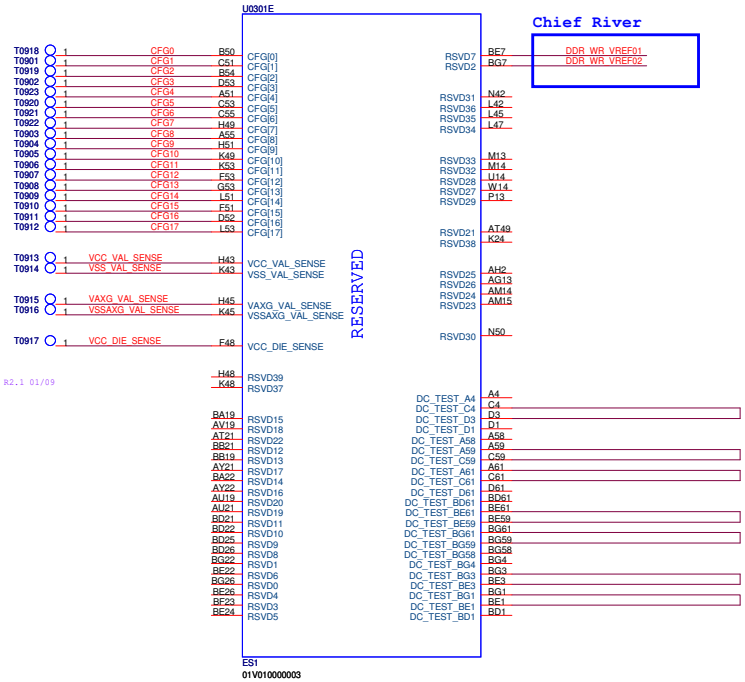
CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

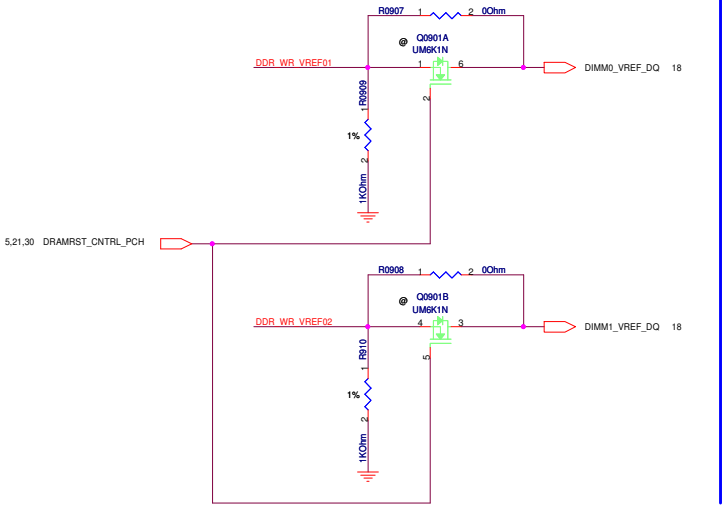
CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training



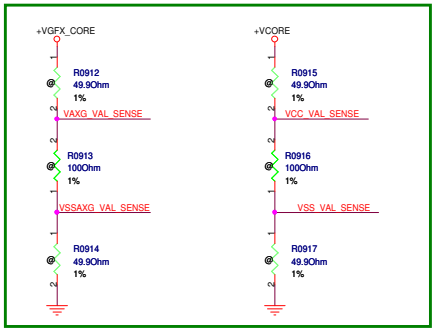


PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



For iFDIM testing
R0912~ R0917 close to pin < 1 inch

R1.1 0512



PEGATRON Title : CPU(7)_RSVD

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 9 of 93

Check Connector

CPU XDP connector

PCH XDP connector

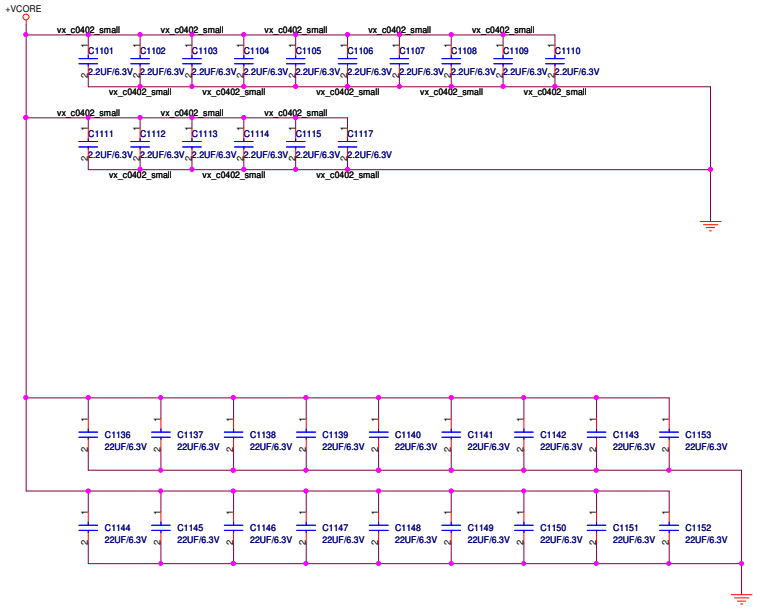
PEGATRON	Title : CPU_PCH_XDP		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 10 of 93		

Chief River

Decoupling guide from Intel PDDG R0.8
+VCORE 2.2uF * 16 pcs
22uF * 12 pcs

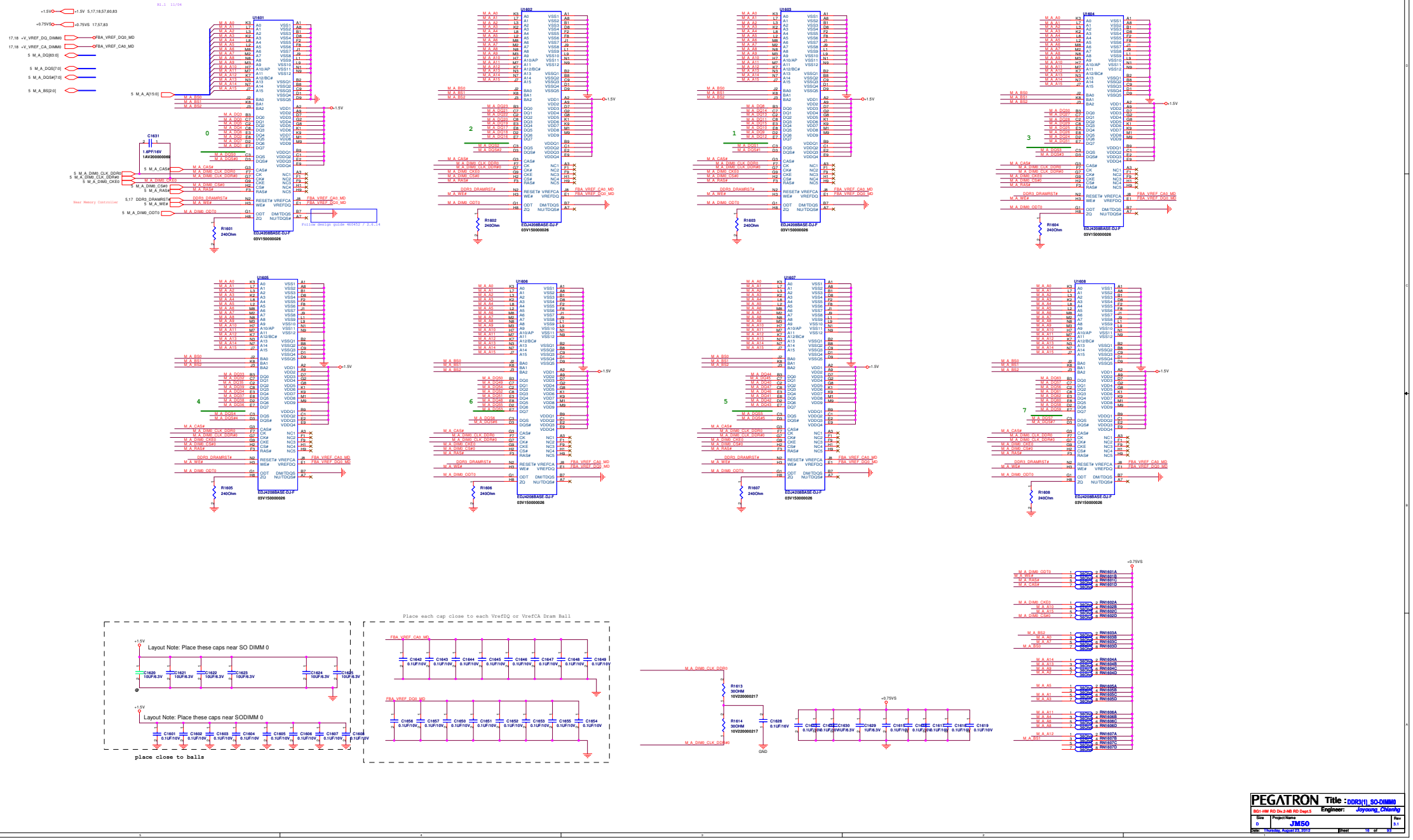
Chief River

+VCORE 2.2uF * 16 pcs
22uF * 18 pcs (power request)



PEGATRON	Title : CPU DECOUPLING	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 11 of 93	

Memory Down CH A



PEGATRON	Title : DDR3(1) SO-DIMM0		
SGI -HW RD Div.2-MB RD Dept.5	Engineer: Joyoung_Chiang		
Size: D	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 16 of 55		

+1.5V → +1.5V 5,16,18,57,60,83

+0.75VS → +0.75VS 16,57,83

+3VS → +3VS 20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+V_VREF_CA_DIMM1 → +V_VREF_CA_DIMM1 16,18

+V_VREF_DQ_DIMM1 → +V_VREF_DQ_DIMM1 16,18

+1.5V — CE1703 220UF/4V @

+1.5V — Layout Note: Place these caps near SO DIMM 1

C1709 10UF/6.3V @ | C1710 10UF/6.3V | C1711 10UF/6.3V @ | C1712 10UF/6.3V | C1713 10UF/6.3V | C1718 10UF/6.3V @

+0.75VS

C1716 1UF/6.3V | C1717 1UF/6.3V | C1719 1UF/6.3V @ | C1730 1UF/6.3V @

5 M_B_A[15:0]

M_B_A0 98 A0 | M_B_A1 97 A1 | M_B_A2 96 A2 | M_B_A3 95 A3 | M_B_A4 92 A4 | M_B_A5 91 A5 | M_B_A6 90 A6 | M_B_A7 86 A7 | M_B_A8 89 A8 | M_B_A9 85 A9 | M_B_A10 107 A10/AP | M_B_A11 84 A11 | M_B_A12 83 A12/BC# | M_B_A13 119 A13 | M_B_A14 80 A14 | M_B_A15 78 A15

J1701A

M_B_DQ[63:0] 5

DQ0 5 M_B_DQ1 | DQ1 7 M_B_DQ5 | DQ2 15 M_B_DQ7 | DQ3 17 M_B_DQ2 | DQ4 4 M_B_DQ4 | DQ5 6 M_B_DQ0 | DQ6 16 M_B_DQ6 | DQ7 18 M_B_DQ3 | DQ8 21 M_B_DQ8 | DQ9 23 M_B_DQ12 | DQ10 33 M_B_DQ10 | DQ11 35 M_B_DQ15 | DQ12 22 M_B_DQ9 | DQ13 24 M_B_DQ13 | DQ14 34 M_B_DQ11 | DQ15 36 M_B_DQ14 | DQ16 39 M_B_DQ16 | DQ17 41 M_B_DQ20 | DQ18 51 M_B_DQ21 | DQ19 53 M_B_DQ17 | DQ20 40 M_B_DQ23 | DQ21 42 M_B_DQ22 | DQ22 50 M_B_DQ19 | DQ23 52 M_B_DQ18 | DQ24 57 M_B_DQ25 | DQ25 59 M_B_DQ28 | DQ26 67 M_B_DQ30 | DQ27 69 M_B_DQ26 | DQ28 56 M_B_DQ29 | DQ29 58 M_B_DQ24 | DQ30 68 M_B_DQ27 | DQ31 70 M_B_DQ31 | DQ32 129 M_B_DQ32 | DQ33 131 M_B_DQ33 | DQ34 141 M_B_DQ38 | DQ35 143 M_B_DQ34 | DQ36 130 M_B_DQ36 | DQ37 132 M_B_DQ37 | DQ38 140 M_B_DQ39 | DQ39 142 M_B_DQ35 | DQ40 147 M_B_DQ44 | DQ41 149 M_B_DQ40 | DQ42 157 M_B_DQ46 | DQ43 159 M_B_DQ41 | DQ44 146 M_B_DQ42 | DQ45 148 M_B_DQ45 | DQ46 158 M_B_DQ47 | DQ47 160 M_B_DQ43 | DQ48 163 M_B_DQ53 | DQ49 165 M_B_DQ52 | DQ50 175 M_B_DQ55 | DQ51 177 M_B_DQ54 | DQ52 164 M_B_DQ49 | DQ53 166 M_B_DQ48 | DQ54 174 M_B_DQ50 | DQ55 176 M_B_DQ51 | DQ56 181 M_B_DQ63 | DQ57 183 M_B_DQ61 | DQ58 191 M_B_DQ57 | DQ59 193 M_B_DQ59 | DQ60 180 M_B_DQ60 | DQ61 182 M_B_DQ56 | DQ62 192 M_B_DQ58 | DQ63 194 M_B_DQ62

0~7 | 8~15 | 16~23 | 24~31 | 32~39 | 40~47 | 48~55 | 56~63

5 M_B_DIM0_CLK_DDR1 → CK1 102
5 M_B_DIM0_CLK_DDR#1 → CK1# 104
5 M_B_DIM0_CLK_DDR0 → CK0 101
5 M_B_DIM0_CLK_DDR#0 → CK0# 103

5 M_B_DIM0_CS#1 → S1# 121
5 M_B_DIM0_CS#0 → S0# 114

5 M_B_DIM0_ODT1 → ODT1 120
5 M_B_DIM0_ODT0 → ODT0 116

5 M_B_WE# → WE# 113
5 M_B_RAS# → RAS# 115
5 M_B_CAS# → CAS# 110

5 M_B_BS2 → BA2 79
5 M_B_BS1 → BA1 108
5 M_B_BS0 → BA0 109

5 M_B_DIM0_CKE1 → CKE1 74
5 M_B_DIM0_CKE0 → CKE0 73

SA1 201
SA0 197

5 M_B_DQS[7:0] → DQS7 188, DQS#7 186, DQS6 171, DQS#6 169, DQS5 154, DQS#5 152, DQS4 137, DQS#4 135, DQS3 64, DQS#3 62, DQS2 47, DQS#2 45, DQS1 29, DQS#1 27, DQS0 12, DQS#0 10

5 M_B_DQS#[7:0]

DM7 187, DM6 170, DM5 153, DM4 136, DM3 63, DM2 46, DM1 28, DM0 11

SCL 202
SDA 200

RESET# 30 → DDR3_DRAMRST# 5,16

M_B_DIM0_CLK_DDR0 — C1720 10PF/50V @ — 150Ohm R1707 — M_B_DIM0_CLK_DDR#0

M_B_DIM0_CLK_DDR1 — C1721 10PF/50V @ — 150Ohm R1708 — M_B_DIM0_CLK_DDR#1

PLACE CLOSE TO SODIMM

SMBus Slave Address: A4H

+3VS — R1709 — SP1703 — 2.10KOhm — SA1

take care if can't boot or S3 issue

DM should connect to GND directly
Design Guide 1.0 P.88 (436735)

28,53,59 SMB_CLK_S → SP1701 — R0402 SMB_CLK_S_CHB
28,53,59 SMB_DAT_S → SP1702 — R0402 SMB_DAT_S_CHB

DDR3_DIMM_204P
12V02GBRM000

H:5.2mm

+1.5V — C1705 0.1UF/16V | C1706 0.1UF/16V | C1707 0.1UF/16V | C1708 0.1UF/16V

Layout Note: Place these caps near SO DIMM 1

J1701B

VDD1 75, VDD3 81, VDD5 87, VDD7 93, VDD9 99, VDD11 105, VDD13 111, VDD15 117, VDD17 123
VDD2 76, VDD4 82, VDD6 88, VDD8 94, VDD10 100, VDD12 106, VDD14 112, VDD16 118, VDD18 124

VSS1 2, VSS3 8, VSS5 13, VSS7 19, VSS9 25, VSS11 31, VSS13 37, VSS15 43, VSS17 48, VSS19 54, VSS21 60, VSS23 65, VSS25 71, VSS27 127, VSS29 133, VSS31 138, VSS33 144, VSS35 150, VSS37 155, VSS39 161, VSS41 167, VSS43 172, VSS45 178, VSS47 184, VSS49 189, VSS51 195
VSS2 3, VSS4 9, VSS6 14, VSS8 20, VSS10 26, VSS12 32, VSS14 38, VSS16 44, VSS18 49, VSS20 55, VSS22 61, VSS24 66, VSS26 72, VSS28 128, VSS30 134, VSS32 139, VSS34 145, VSS36 151, VSS38 156, VSS40 162, VSS42 168, VSS44 173, VSS46 179, VSS48 185, VSS50 190, VSS52 196

T1701 — PM_EXTTS#0_DIM_B — Reserve

EVENT# 198
TEST 125
NC1 77
NC2 122

GND1 207, GND2 208
NP_NC1 205, NP_NC2 206
VTT1 203, VTT2 204 → +0.75VS

VREFCA 126
VREFDQ 1
VDDSPD 199 → +3VS

+V_VREF_CA_DIMM1 — C1724 2.2UF/6.3V @ — C1723 0.1UF/16V

+V_VREF_DQ_DIMM1 — C1722 2.2UF/6.3V @ — C1725 0.1UF/16V

C1715 0.1UF/16V — C1714 2.2UF/6.3V @

Frank
20110513 VREFCA and VREFDQ need to separate
It follow EVEREST and Intel spec.

DDR3_DIMM_204P
12V02GBRM000

PEGATRON Title : DDR3(2)_SO-DIMM1

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

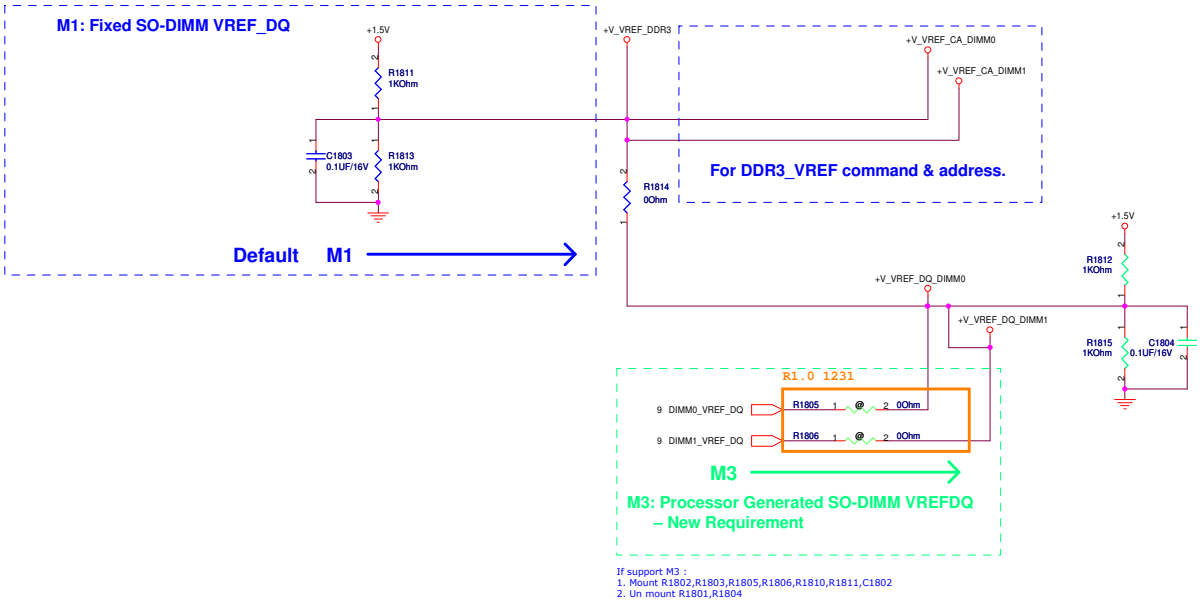
Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 17 of 93

DDR3 Vref

+1.5V +1.5V 5,16,17,57,60,83
+V_VREF_CA_DIMM0 +V_VREF_CA_DIMM0 16,17
+V_VREF_DQ_DIMM0 +V_VREF_DQ_DIMM0 16,17

+3V +3V 24,45,57,59,61,91
+5VSUS +5VSUS 51,57,59,91
+5VA +5VA 37,60,81,91



If support M3 :
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804

PEGATRON Title : DDR3(3)_CA/DQ Voltage

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 18 of 93

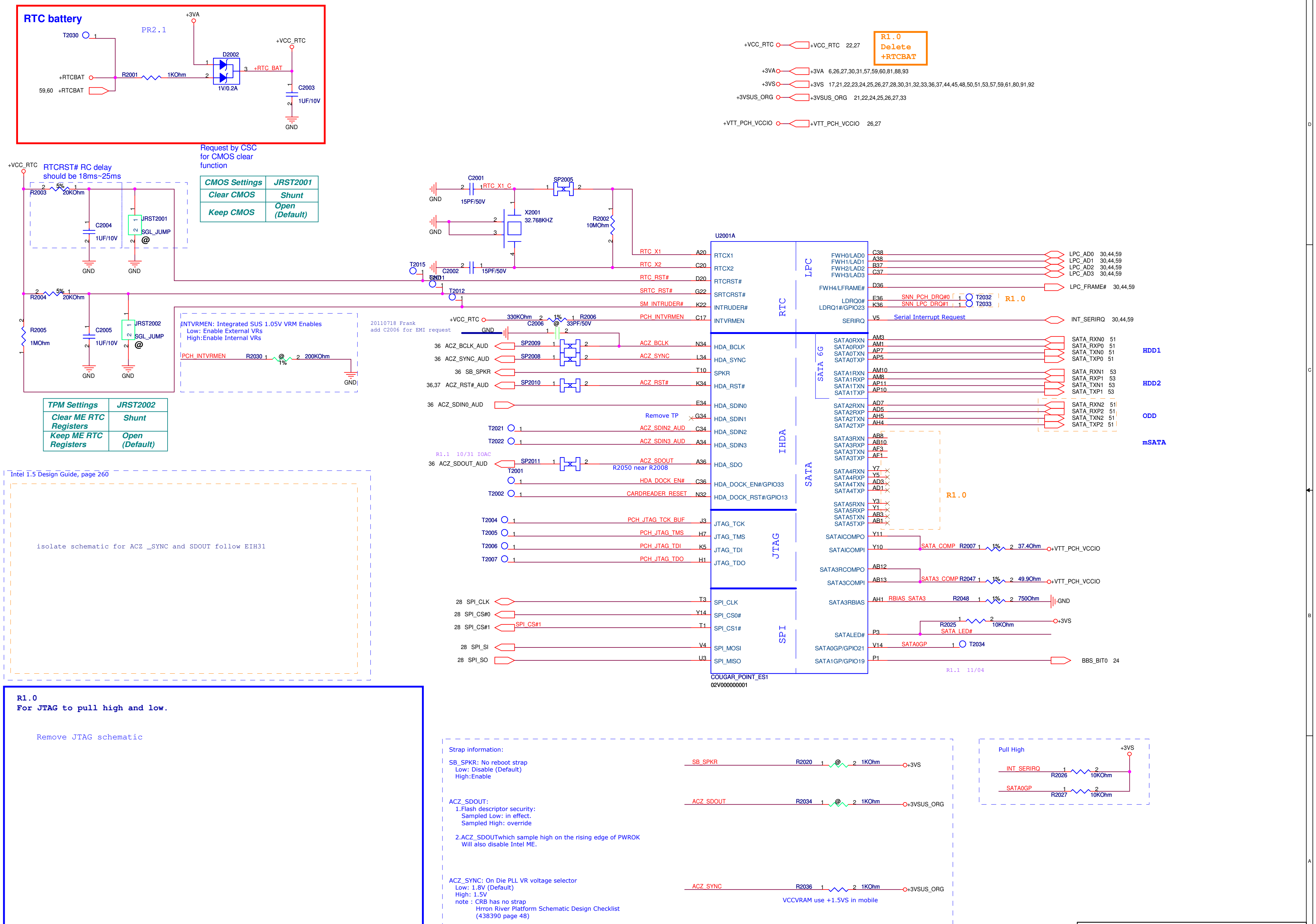
R1.4--2

PEGATRON Title : VID Controller

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 19 of 93



RTC battery
PR2.1
+3VA
T2030
+VCC_RTC
D2002
+RTCBAT
R2001 1KOhm
+RTC_BAT
C2003
59,60 +RTCBAT
1V/0.2A
1UF/10V
GND
Request by CSC for CMOS clear function
RTCRST# RC delay should be 18ms~25ms
R2003 20KOhm
C2004 1UF/10V
JRST2001 SGL_JUMP
R2004 20KOhm
R2005 1MOhm
C2005 1UF/10V
JRST2002 SGL_JUMP
INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs
PCH_INTVRMEN R2030 200KOhm
20110718 Frank
add C2006 for EMI request
C2001 15PF/50V RTC_X1_C
SP2005
X2001 32.768KHZ
R2002 10MOhm
C2002 15PF/50V
T2015 T2011 T2012
+VCC_RTC 330KOhm R2006 C2006 33PF/50V
U2001A
RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
36 ACZ_BCLK_AUD SP2009 ACZ_BCLK N34 HDA_BCLK
36 ACZ_SYNC_AUD SP2008 ACZ_SYNC L34 HDA_SYNC
36 SB_SPKR T10 SPKR
36,37 ACZ_RST#_AUD SP2010 ACZ_RST# K34 HDA_RST#
36 ACZ_SDIN0_AUD E34 HDA_SDIN0
Remove TP G34 HDA_SDIN1
T2021 ACZ_SDIN2_AUD C34 HDA_SDIN2
T2022 ACZ_SDIN3_AUD A34 HDA_SDIN3
R1.1 10/31 IOAC
36 ACZ_SDOUT_AUD SP2011 ACZ_SDOUT A36 HDA_SDO
T2001 R2050 near R2008
HDA_DOCK_EN# C36 HDA_DOCK_EN#/GPIO33
T2002 CARDREADER_RESET N32 HDA_DOCK_RST#/GPIO13
T2004 PCH_JTAG_TCK_BUF J3 JTAG_TCK
T2005 PCH_JTAG_TMS H7 JTAG_TMS
T2006 PCH_JTAG_TDI K5 JTAG_TDI
T2007 PCH_JTAG_TDO H1 JTAG_TDO
28 SPI_CLK T3 SPI_CLK
28 SPI_CS#0 Y14 SPI_CS0#
28 SPI_CS#1 SPI_CS#1 T1 SPI_CS1#
28 SPI_SI V4 SPI_MOSI
28 SPI_SO U3 SPI_MISO
COUGAR_POINT_ES1
02V000000001
RTC LPC IHDA JTAG SPI SATA SATA 6G
FWH0/LAD0 C38 LPC_AD0 30,44,59
FWH1/LAD1 A38 LPC_AD1 30,44,59
FWH2/LAD2 B37 LPC_AD2 30,44,59
FWH3/LAD3 C37 LPC_AD3 30,44,59
FWH4/LFRAME# D36 LPC_FRAME# 30,44,59
LDRQ0# E36 SNN_PCH_DRQ#0 T2032
LDRQ1#/GPIO23 K36 SNN_LPC_DRQ#1 T2033
R1.0
SERIRQ V5 Serial Interrupt Request INT_SERIRQ 30,44,59
SATA0RXN AM3 SATA_RXN0 51
SATA0RXP AM1 SATA_RXP0 51
SATA0TXN AP7 SATA_TXN0 51
SATA0TXP AP5 SATA_TXP0 51
HDD1
SATA1RXN AM10 SATA_RXN1 53
SATA1RXP AM8 SATA_RXP1 53
SATA1TXN AP11 SATA_TXN1 53
SATA1TXP AP10 SATA_TXP1 53
HDD2
SATA2RXN AD7 SATA_RXN2 51
SATA2RXP AD5 SATA_RXP2 51
SATA2TXN AH5 SATA_TXN2 51
SATA2TXP AH4 SATA_TXP2 51
ODD
mSATA
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
R1.0
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R2007 37.4Ohm +VTT_PCH_VCCIO
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R2047 49.9Ohm +VTT_PCH_VCCIO
SATA3RBIAS AH1 RBIAS_SATA3 R2048 750Ohm GND
R2025 10KOhm +3VS
SATALED# P3 SATA_LED#
SATA0GP/GPIO21 V14 SATA0GP T2034
SATA1GP/GPIO19 P1 BBS_BIT0 24
R1.1 11/04
+VCC_RTC +VCC_RTC 22,27
R1.0 Delete +RTCBAT
+3VA +3VA 6,26,27,30,31,57,59,60,81,88,93
+3VS +3VS 17,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3VSUS_ORG +3VSUS_ORG 21,22,24,25,26,27,33
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 26,27
Intel 1.5 Design Guide, page 260
isolate schematic for ACZ _SYNC and SDOUT follow EIH31
Strap information:
SB_SPKR R2020 1KOhm +3VS
ACZ_SDOUT R2034 1KOhm +3VSUS_ORG
ACZ_SYNC R2036 1KOhm +3VSUS_ORG
VCCVRAM use +1.5VS in mobile
Pull High +3VS
INT_SERIRQ R2026 10KOhm
SATA0GP R2027 10KOhm

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist
(438390 page 48)

R1.0
For JTAG to pull high and low.

Remove JTAG schematic

PEGATRON Title : PCH(1)_SATA,IHDA,RTC,LPC
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C Project Name JM50 Rev 3.1
Date: Thursday, August 23, 2012 Sheet 20 of 93

Frank
0513_Add USB3.0 and Card Reader PCIE and CLKRQ

Frank
0517_Add 3G PCIE and CLKRQ in Port3.

+3VS +3VS 17,20,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+3VSUS_ORG +3VSUS_ORG 20,22,24,25,26,27,33

Joyoung R1.0

59 PCIE_RXN1_CR
59 PCIE_RXP1_CR
59 PCIE_TXN1_CR
59 PCIE_TXP1_CR
C2112 0.1UF/16V PCIE_TXN1_CR_C
C2114 0.1UF/16V PCIE_TXP1_CR_C

53 PCIE_RXN2_WLAN
53 PCIE_RXP2_WLAN
53 PCIE_TXN2_WLAN
53 PCIE_TXP2_WLAN
C2103 0.1UF/16V PCIE_TXN2_WLAN_C
C2104 0.1UF/16V PCIE_TXP2_WLAN_C

53 PCIE_RXN3_mSATA
53 PCIE_RXP3_mSATA
53 PCIE_TXN3_mSATA
53 PCIE_TXP3_mSATA

33 PCIE_RXN4_GLAN
33 PCIE_RXP4_GLAN
33 PCIE_TXN4_GLAN
33 PCIE_TXP4_GLAN
C2110 0.1UF/16V PCIE_TXN4_GLAN_C
C2111 0.1UF/16V PCIE_TXP4_GLAN_C

R1.1
remove /niAMT remark

T2101 T2102 T2108 T2109 PCIE_TXN5_CR_C PCIE_TXP5_CR_C
T2104 T2105 T2106 T2107 PCIE_TXN6_USB30_C PCIE_TXP6_USB30_C

U2001B

PCI-E*
BG34 PERn1 / BJ34 PERp1 / AT32 PETn1 / AU32 PETp1
BE34 PERn2 / BE34 PERp2 / BB32 PETn2 / AY32 PETp2
BG36 PERn3 / BJ36 PERp3 / AY34 PETn3 / AU34 PETp3
BF36 PERn4 / BE36 PERp4 / AY34 PETn4 / BB34 PETp4
BG37 PERn5 / BH37 PERp5 / AY36 PETn5 / BB36 PETp5
BJ38 PERn6 / BG38 PERp6 / AU36 PETn6 / AV36 PETp6
BG40 PERn7 / BJ40 PERp7 / AY40 PETn7 / BB40 PETp7
BE38 PERn8 / BC38 PERp8 / AW38 PETn8 / AY38 PETp8

SMBUS
SMBALERT#/GPIO11 E12 EXT_SCI# → EXT_SCI# 30,59
SMBCLK H14 SCL_3A → SCL_3A 28
SMBDATA C9 SDA_3A → SDA_3A 28
SML0ALERT#/GPIO60 A12 DRAMRST_CNTRL_PCH_R R2161 /NON_DS3 2 0Ohm → DRAMRST_CNTRL_PCH 5,9,30
SML0CLK C8 SML0_CLK → T2133
SML0DATA G12 SML0_DAT → T2134
SML1ALERT#/PCHHOT#/GPIO74 C13 SML1ALERT#
SML1CLK/GPIO58 E14 SML1_CLK → SML1_CLK 28
SML1DATA/GPIO75 M16 SML1_DAT → SML1_DAT 28
R2.0 12/14
R1.0
To EC

Controller Link
CL_CLK1 M7
CL_DATA1 T11
CL_RST1# P10

CLOCKS
CLKOUT_PCIE0N Y40 / CLKOUT_PCIE0P Y39 100MHz
CLK_REQ0# → PCIECLKRQ0#/GPIO73 J2
CLKOUT_PCIE1N AB49 / CLKOUT_PCIE1P AB47 100MHz
CLK_REQ1# → PCIECLKRQ1#/GPIO18 M1
CLKOUT_PCIE2N AA48 / CLKOUT_PCIE2P AA47 100MHz
CLK_REQ2# → PCIECLKRQ2#/GPIO20 V10
CLKOUT_PCIE3N Y37 / CLKOUT_PCIE3P Y36 100MHz
CLK_REQ3# → PCIECLKRQ3#/GPIO25 A8
CLKOUT_PCIE4N Y43 / CLKOUT_PCIE4P Y45 100MHz
CLK_REQ4# → PCIECLKRQ4#/GPIO26 L12
CLKOUT_PCIE5N V45 / CLKOUT_PCIE5P V46 100MHz
CLK_REQ5# → PCIECLKRQ5#/GPIO44 L14
CLKOUT_PEG_B_N AB42 / CLKOUT_PEG_B_P AB40 100MHz
CLK_REQ_PEG_B# → PEG_B_CLKRQ#/GPIO56 E6
CLKOUT_PCIE6N Y40 / CLKOUT_PCIE6P V42 100MHz
CLK_REQ6# → PCIECLKRQ6#/GPIO45 T13
CLKOUT_PCIE7N V38 / CLKOUT_PCIE7P V37 100MHz
CLK_REQ7# → PCIECLKRQ7#/GPIO46 K12
CLKOUT_ITPXDP_N AK14 / CLKOUT_ITPXDP_P AK13 100MHz
Remove XDP.

COUGAR_POINT_ES1

PEG_A_CLKRQ#/GPIO47 M10 CLK_REQ_PEG_A# → CLKREQ_PEG# 70
CLKOUT_PEG_A_N AB37 CLK_PCIE_PEG#_PCH_L R2103 NB_R0402_20MIL_SMALL → CLK_PCIE_PEG#_PCH 70
CLKOUT_PEG_A_P AB38 CLK_PCIE_PEG_PCH_L R2104 NB_R0402_20MIL_SMALL → CLK_PCIE_PEG_PCH 70
CLKOUT_DMI_N AV22 → CLK_EXP_N 4
CLKOUT_DMI_P AU22 → CLK_EXP_P 4
CLKOUT_DP_N AM12 CLK_DP_N → CLK_DP_N 4
CLKOUT_DP_P AM13 CLK_DP_P → CLK_DP_P 4
CLKIN_DMI_N BF18 CLK_BUF_EXP_N
CLKIN_DMI_P BE18 CLK_BUF_EXP_P
CLKIN_GND1_N BJ30 CLK_BUF_CPYCLK_N
CLKIN_GND1_P BG30 CLK_BUF_CPYCLK_P
CLKIN_DOT_96N G24 CLK_BUF_DOT96_N
CLKIN_DOT_96P E24 CLK_BUF_DOT96_P
CLKIN_SATA_N AK7 CLK_BUF_CKSSCD_N
CLKIN_SATA_P AK5 CLK_BUF_CKSSCD_P
REFCLK14IN K45 CLK_BUF_REF14
CLKIN_PCILOOPBACK H45 → CLK_PCI_FB 24
XTAL25_IN V47 XTAL25_IN
XTAL25_OUT V49 XTAL25_OUT
XCLK_COMP Y47 XCLK_COMP R2106 90.9Ohm → +VCCDIFFCLKN

FLEX CLOCKS
CLKOUTFLEX0/GPIO64 K43 → SYSRAM00
CLKOUTFLEX1/GPIO65 F47 → SYSRAM01
CLKOUTFLEX2/GPIO66 H47 → SYSRAM02
CLKOUTFLEX3/GPIO67 K49 → SYSRAM03

02V000000001

Joyoung R1.0
modify CLK_REQ

25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock gereration in Integrated Graphics platforms

C2101 10PF/50V
X2103 25MHZ
C2102 10PF/50V
R2142 10Ohm
SP2111

CLOCK TERMINATION FOR FCIM
Default power-on mode is ICC.
CLK_BUF_CPYCLK_N RN2108B
CLK_BUF_CPYCLK_P RN2108A
CLK_BUF_EXP_N RN2109B
CLK_BUF_EXP_P RN2109A
CLK_BUF_DOT96_N RN2110B
CLK_BUF_DOT96_P RN2110A
CLK_BUF_CKSSCD_N RN2111B
CLK_BUF_CKSSCD_P RN2111A
CLK_BUF_REF14 R2116 10KOhm

R1.1
S3 RAM reset CTRL
R2.0 12/20
R2.0 12/14
EXT_SCI# R2117 10KOhm
SCL_3A RN2103B 2.2KOhm
SDA_3A RN2103A 2.2KOhm
DRAMRST_CNTRL_PCH_R R2120 10KOhm
SML0_CLK RN2104B 2.2KOhm
SML0_DAT RN2104A 2.2KOhm
SML1_CLK RN2105A 2.2KOhm
SML1_DAT RN2105B 2.2KOhm
SML1ALERT# R2125 10KOhm **UNSTUFF**

PCH CLKREQ Setting:
Not connected to device.
R1.0 0118
CLK_REQ0# R2150 10KOhm **UNSTUFF**
CLK_REQ5# R2139 10KOhm **UNSTUFF**
CLK_REQ7# RN2107B 10KOhm
CLK_REQ_PEG_B# RN2107A 10KOhm
CLK_REQ6# R2143 10KOhm **UNSTUFF**

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
Eric Fang to Alan Chien on 11/15/2010
CLK_REQ1# R2133 10KOhm
CLK_REQ2# R2128 10KOhm
CLK_REQ3# R2151 10KOhm
CLK_REQ4# R2135 10KOhm
CLK_REQ_PEG_A# R2140 10KOhm
CLK_REQ_PEG_A# R2141 10KOhm
CLK_REQ3# R2148 10KOhm
CLK_REQ4# R2146 10KOhm
CLK_REQ1# R2138 10KOhm
CLK_REQ2# R2145 10KOhm

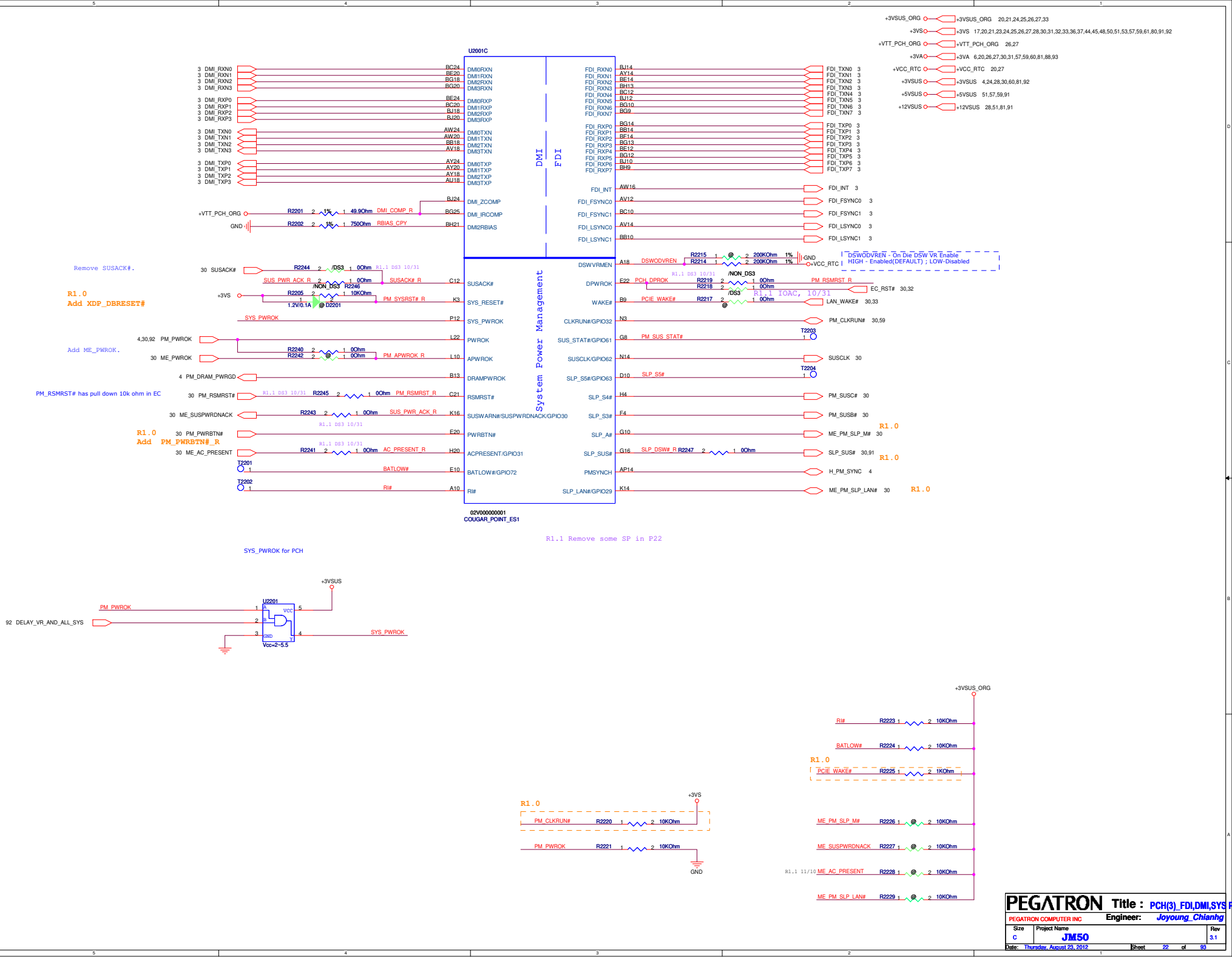
R2.0
Modify RAM Strap PIN
R2.0 12/15
R2144 10KOhm @
R2152 10KOhm /2G
R2154 10KOhm /E
R2156 10KOhm /M\1600
R2149 10KOhm
R2153 10KOhm /4G
R2155 10KOhm /M\H
R2157 10KOhm /E\H
SYSRAM00 SYSRAM01 SYSRAM02 SYSRAM03

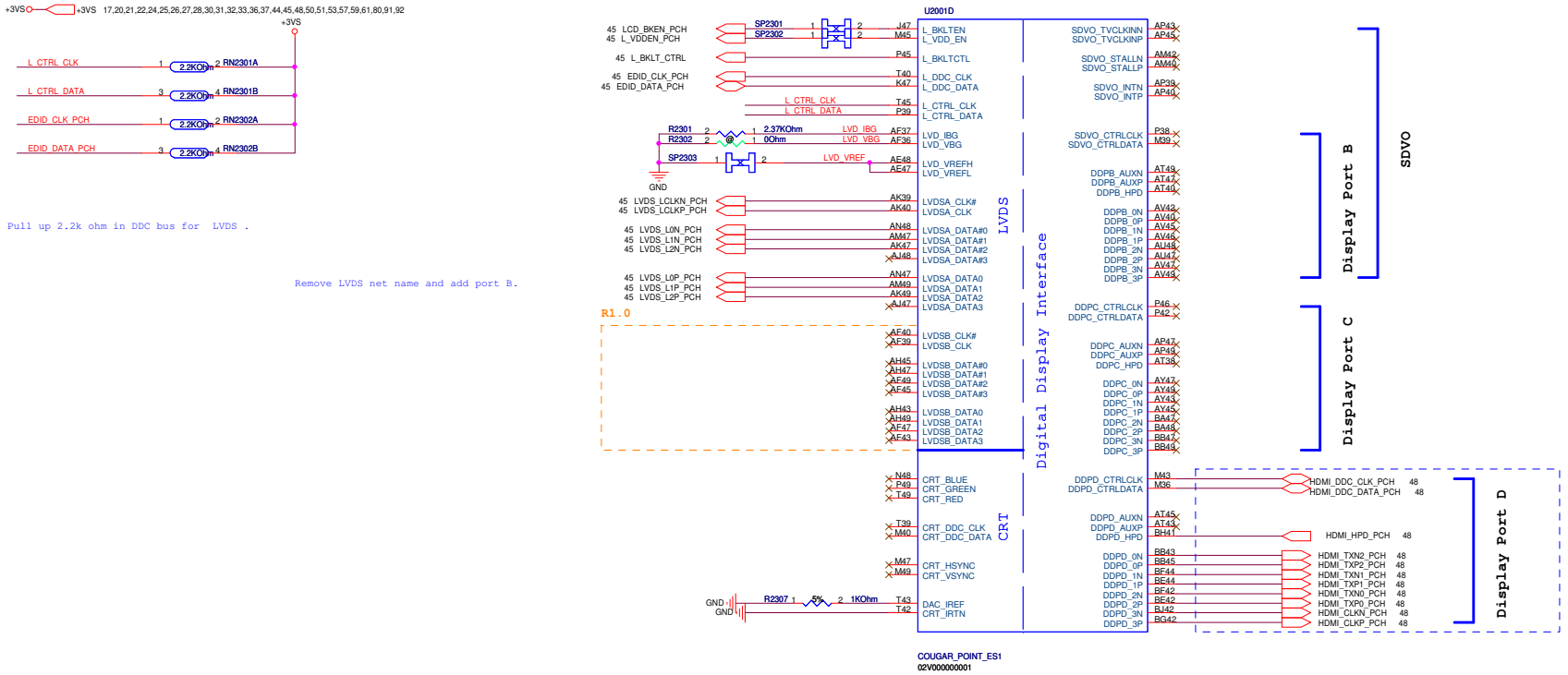
Joyoung R2.0
add GPIO Table for on board RAM Strap

On Board RAM Setting

GPIO67 GPIO66 GPIO65 GPIO64	On Board RAM Setting
0000	No on board RAM
0001	Micron 1333MHz 4GB
0010	Elpida 1333MHz 4GB
0110	Elpida 1333MHz 2GB
0101	Micron 1333MHz 2GB
0100	Hynix 1333MHz 2GB
XXXX	TBD
1000	Common Definition 1333MHz 4GB
1001	Common Definition 1600MHz 4GB
0111	Elpida 1600MHz 2GB

PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 21 of 93


U2001C
DMI
FDI
System Power Management
DMI0RXN
DMI1RXN
DMI2RXN
DMI3RXN
DMI0RXP
DMI1RXP
DMI2RXP
DMI3RXP
DMI0TXN
DMI1TXN
DMI2TXN
DMI3TXN
DMI0TXP
DMI1TXP
DMI2TXP
DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
DMI2RBIAS
FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
SLP_LAN#/GPIO29
DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
02V000000001
COUGAR_POINT_ES1
+3VSUS_ORG
+3VS
+VTT_PCH_ORG
+3VA
+VCC_RTC
+5VSUS
+12VSUS
DMI_COMP_R
RBIAS_CPY
DSWODVREN
PCH_DPROK
PCIE_WAKE#
PM_CLKRUN#
PM_SUS_STAT#
SUSCLK
SLP_S5#
PM_SUSC#
PM_SUSB#
ME_PM_SLP_M#
SLP_SUS#
H_PM_SYNC
ME_PM_SLP_LAN#
PM_RSMRST_R
EC_RST#
LAN_WAKE#
SUSACK# R
PM_SYSRST# R
PM_APWROK_R
PM_RSMRST_R
SUS_PWR_ACK_R
AC_PRESENT_R
BATLOW#
RI#
SLP_DSW#_R
DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled
Remove SUSACK#.
R1.0
Add XDP_DBRESET#
Add ME_PWROK.
PM_RSMRST# has pull down 10k ohm in EC
R1.0
Add PM_PWRBTN#_R
R1.1 IOAC, 10/31
R1.1 Remove some SP in P22
SYS_PWROK for PCH
U2201
PM_PWROK
DELAY_VR_AND_ALL_SYS
SYS_PWROK
Vcc=2~5.5
PM_CLKRUN#
PM_PWROK
ME_PM_SLP_M#
ME_SUSPWRDNACK
ME_AC_PRESENT
ME_PM_SLP_LAN#
PCIE_WAKE#
GND



CRT Disable: (For discrete graphic)

1. **NC:**
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. **1-kΩ ±0.5% pull-down to GND:**
   DAC_IREF
3. **Connected to GND:**
   CRT_ITRN
4. **Connect to +V3.3:**
   VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. **NC:**
   ALL

LVDS Disable: (For discrete graphic)

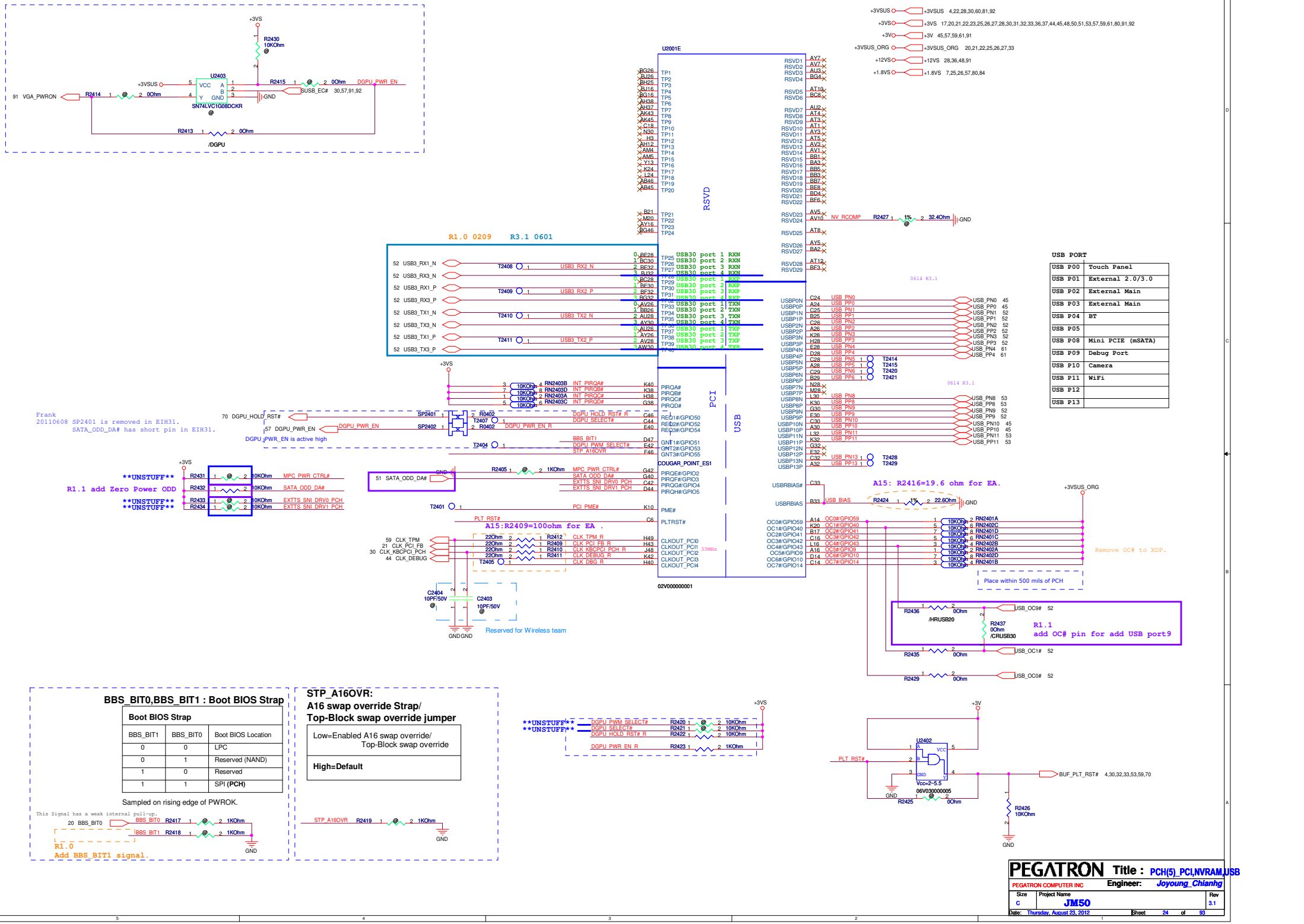
1. **NC:**
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. **Connected to GND:**
   VccALVDS,VccTX_LVDS

PEGATRON Title : PCH(4)_DP,LVDS,CRT

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 23 of 93


+3VS
R2430 10KOhm
U2403
SN74LVC1G08DCKR
R2414 0Ohm
R2415 0Ohm
R2413 0Ohm
91 VGA_PWRON
DGPU_PWR_EN
SUSB_EC# 30,57,91,92
/DGPU
+3VSUS 4,22,28,30,60,81,92
+3VS 17,20,21,22,23,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3V 45,57,59,61,91
+3VSUS_ORG 20,21,22,25,26,27,33
+12VS 28,36,48,91
+1.8VS 7,25,26,57,80,84
U2001E
RSVD
PCI
USB
COUGAR_POINT_ES1
02V000000001
NV_RCOMP R2427 32.4Ohm
R1.0 0209 R3.1 0601
USB3_RX1_N T2408 USB3_RX2_N
USB3_RX3_N
USB3_RX1_P T2409 USB3_RX2_P
USB3_RX3_P
USB3_TX1_N T2410 USB3_TX2_N
USB3_TX3_N
USB3_TX1_P T2411 USB3_TX2_P
USB3_TX3_P
USB PORT
USB P00 Touch Panel
USB P01 External 2.0/3.0
USB P02 External Main
USB P03 External Main
USB P04 BT
USB P05
USB P08 Mini PCIE (mSATA)
USB P09 Debug Port
USB P10 Camera
USB P11 WiFi
USB P12
USB P13
0614 R3.1
Frank
20110608 SP2401 is removed in EIH31.
SATA_ODD_DA# has short pin in EIH31.
DGPU_PWR_EN is active high
DGPU_HOLD_RST# SP2401 R0402
DGPU_PWR_EN SP2402 R0402
T2407 T2404
RN2403B INT_PIRQA#
RN2403D INT_PIRQB#
RN2403A INT_PIRQC#
RN2403C INT_PIRQD#
UNSTUFF
R1.1 add Zero Power ODD
R2431 10KOhm MPC_PWR_CTRL#
R2432 10KOhm SATA_ODD_DA#
R2433 10KOhm EXTTS_SNI_DRV0_PCH
R2434 10KOhm EXTTS_SNI_DRV1_PCH
51 SATA_ODD_DA#
R2405 1KOhm
A15:R2409=100ohm for EA .
59 CLK_TPM
21 CLK_PCI_FB
30 CLK_KBCPCI_PCH
44 CLK_DEBUG
22Ohm R2412 CLK_TPM_R
22Ohm R2409 CLK_PCI_FB_R
22Ohm R2410 CLK_KBCPCI_PCH_R
22Ohm R2411 CLK_DEBUG_R
T2405
C2404 10PF/50V
C2403 10PF/50V
GND GND
Reserved for Wireless team
A15: R2416=19.6 ohm for EA.
USB_BIAS R2424 22.6Ohm
+3VSUS_ORG
Remove OC# to XDP.
Place within 500 mils of PCH
R2436 0Ohm /HRUSB20
R2437 0Ohm /CRUSB30
R1.1 add OC# pin for add USB port9
R2435 0Ohm
R2429 0Ohm
USB_OC9# 52
USB_OC1# 52
USB_OC0# 52
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT1 BBS_BIT0 Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 Reserved
1 1 SPI (PCH)
Sampled on rising edge of PWROK.
This Signal has a weak internal pull-up.
20 BBS_BIT0 R2417 1KOhm
BBS_BIT1 R2418 1KOhm
R1.0
Add BBS_BIT1 signal.
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
Low=Enabled A16 swap override/
Top-Block swap override
High=Default
STP_A16OVR R2419 1KOhm
UNSTUFF
DGPU_PWM_SELECT# R2420 10KOhm
DGPU_SELECT# R2421 10KOhm
DGPU_HOLD_RST# R R2422 10KOhm
DGPU_PWR_EN R R2423 1KOhm
U2402
PLT_RST#
Vcc=2~5.5
06V030000005
R2425 0Ohm
R2426 10KOhm
BUF_PLT_RST# 4,30,32,33,53,59,70
PEGATRON
Title : PCH(5)_PCI,NVRAM,USB
PEGATRON COMPUTER INC
Engineer: Joyoung_Chianhg
Size C
Project Name JM50
Rev 3.1
Date: Thursday, August 23, 2012
Sheet 24 of 93

+3VS +3VS 17,20,21,22,23,24,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+3VSUS +3VSUS 4,22,24,28,30,60,81,92

+3VSUS_ORG +3VSUS_ORG 20,21,22,24,26,27,33

R1.0

Add PM_LANPHY_EN

Add HOST_ALERT#1_R.

DGPU_PWROK has 100 ms software delay , no hardware delay requirement

Reserve PCH_GPIO24

Add SATA_ODD_PRSNT#_R and FDI_OVRVLTG.

Add CRIT_TEMP_REP#_R.

Remove CRIT_PCH_GPIO0_R to XDP

U2001F

GPIO0 T7 BMBUSY#/GPIO0
45 TPN_INT# JM50_T 05/08 1 /TPN 0Ohm 2 R2522 GPIO1 A42 TACH1/GPIO1
T2503 1 DGPU_HPD_INTR# H36 TACH2/GPIO6
GPIO7 E38 TACH3/GPIO7
USB30_EXT_SMI# C10 GPIO8
33 LAN_LPWR SP2505 1 2 R0402 PM_LANPHY_EN C4 LAN_PHY_PWR_CTRL/GPIO12
30,44 EXT_SMI# SP2501 1 2 HOST_ALERT#1_R G2 GPIO15
DGPU_PRSNT# U2 SATA4GP/GPIO16
87,91 DGPU_PWROK DGPU_PWROK D40 TACH0/GPIO17
T2141 1 WLAN_LED T5 SCLOCK/GPIO22
53 AOAC_ON AOAC_ON E8 GPIO24/MEM_LED
R1.0 0106 R1.1 Change WLAN_ON to WLAN_ON_PCH GPIO27 E16 GPIO27
Frank 30,53 RF_ON 0Ohm 1 @ 2 R2517 WLAN_ON_R P8 GPIO28
0531 EE define GPIO for BROADCOM LAN chip. STP_PCI# K1 STP_PCI#/GPIO34
T2506 1 SATA_PWR_EN#1_R K4 GPIO35
51 SATA_ODD_PRSNT#_R SATA_ODD_PRSNT#_R V8 SATA2GP/GPIO36
R1.1 add Zero Power ODD FDI_OVRVLTG M5 SATA3GP/GPIO37
PCB_ID0 N2 SLOAD/GPIO38
R2.0 12/13 PCB_ID1 M3 SDATAOUT0/GPIO39
30,53,61 BT_ON BT_ON 0Ohm 1 @ 2 R2523 V13 SDATAOUT1/GPIO48
R1.1 DS3 10/31 T2512 1 PCH_ALERT# V3 SATA5GP/GPIO49
T2511 1 BT_LED D6 GPIO57

GPIO

TACH4/GPIO68 C40 SATA_ODD_PWRGT
TACH5/GPIO69 B41
TACH6/GPIO70 C41
TACH7/GPIO71 A40

R1.1 add Zero Power ODD
SATA_ODD_PWRGT 51
T2508 T2507 T2505
UNSTUFF
UNSTUFF
UNSTUFF
R1.1 11/04

Frank
20110608 H_THRMTRIP# is not connected pull up resister but EIH 31 does not.

CPU/MISC

A20GATE P4 A20GATE 30
PECI AU16 H_PECI_R 0Ohm 1 @ 2 R2514 43Ohm 1 2 R2515 H_PECI 4 H_PECI_EC 30
RCIN# P5 RCIN# 30
PROCPWRGD AY11 H_CPUPWRGD 4
THRMTRIP# AY10 PM_THRMTRIP# 390Ohm 1 1% 2 R2516 H_THRMTRIP# 4,32
INIT3_3V# T14 INIT3_3V# 1 T2504
DF_TVS AY1 NV_CLE R2502 1 2 1KOhm H_SNB_IVB# 4
R2503 1 2 2.2KOhm +1.8VS
R1.0

TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37
GND

TS Signal Disable Guideline
TS_VSS[1:4] should pull down to GND
Design Guide 0.9 (436735)

NCTF

Vss_NCTF1 A4
Vss_NCTF2 A44
Vss_NCTF3 A45
Vss_NCTF4 A46
Vss_NCTF5 A5
Vss_NCTF6 A6
Vss_NCTF7 R3
Vss_NCTF8 B47
Vss_NCTF9 BD1
Vss_NCTF10 BD49
Vss_NCTF11 BE1
Vss_NCTF12 BE49
Vss_NCTF13 BF1
Vss_NCTF14 BF49
Vss_NCTF15 BG2
Vss_NCTF16 BG48
Vss_NCTF17 BH3
Vss_NCTF18 BH47
Vss_NCTF19 BJ4
Vss_NCTF20 BJ44
Vss_NCTF21 BJ45
Vss_NCTF22 BJ46
Vss_NCTF23 BJ5
Vss_NCTF24 BJ6
Vss_NCTF25 C2
Vss_NCTF26 C48
Vss_NCTF27 D1
Vss_NCTF28 D49
Vss_NCTF29 E1
Vss_NCTF30 E49
Vss_NCTF31 F1
Vss_NCTF32 F49

COUGAR_POINT_ES1 02V000000001

Frank
0502 NO BT module, but the GPIO control pin will conntact to page 55. It supports combo card.

Frank
0502 No WLAN LED,so GPIO pin change test point

Frank
0504 CRIT_TEMP_REP#_R change net name CRIT_TEMP_REP# and contact to EC(follow BIC50)

Frank
0516 Remove SATA_DET#4_R to XDP

Frank
0516 Remove PLL_ODVR_EN and SATA_PWR_EN#1_R to XDP

Frank
0516 Remove FDI_OVRVLTG to XDP

Frank
0516 Remove CRIT_TEMP_REP#_R to XDP

R1.0 0111

+3VS +3VS
R2.0 12/22
/HR_IOAC R2525 10KOhm R2527 10KOhm /DS3 PCB_ID0 PCB_ID1
/CR R2526 10KOhm R2528 10KOhm /NON_DS3
GND GND

+3VSUS_ORG

R1.0 Intel Comments

UNSTUFF EXT_SMI# R2529 1 2 1KOhm
UNSTUFF USB30_EXT_SMI# R2531 2 @ 1 10KOhm
UNSTUFF PM_LANPHY_EN R2538 2 @ 1 10KOhm
AOAC_ON R2541 2 @ 1 10KOhm

Joyoung R1.0
Joyoung R1.1
remove /niAMT remark

Joyoung R1.0
mount if suppot AOAC

RCIN# has pull high at EC side
UNSTUFF DGPU_HPD_INTR# R2534 2 @ 1 10KOhm
DGPU_PWROK R2539 2 1 10KOhm

R1.0

Unused GPIO
GPIO0 R2536 2 1 10KOhm
UNSTUFF STP_PCI# R2537 2 1 10KOhm
UNSTUFF WLAN_LED R2542 2 @ 1 10KOhm
UNSTUFF GPIO27 R2548 2 @ 1 10KOhm
#438390 Checklist
GND

DGPU_PWROK R2540 2 @ 1 10KOhm
GPIO1 100KOhm 2 @ 1 R2545
JM50_T 05/11
GND

Joyoung R1.0
+3VS
DGPU_PRSNT# R2126 1 /UMA 2 10KOhm
DGPU_PRSNT# R2134 1 /DGPU 2 10KOhm
GND

Joyoung R1.0
for BIOS detect Panel
+3VS
GPIO7 R2549 2 /LVDS 1 10KOhm
GPIO7 R2547 2 eDP 1 10KOhm
GND

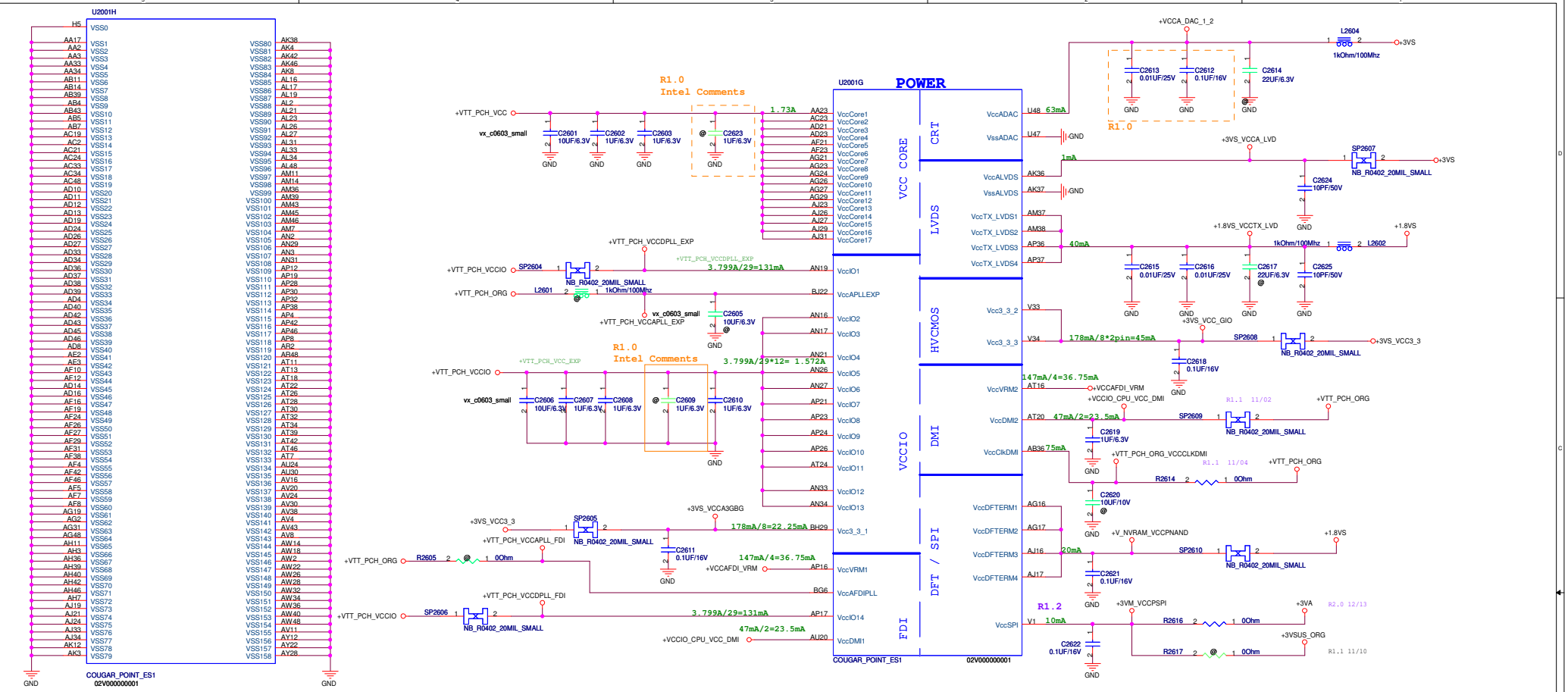
+3VS R2518 1 1% 2 1KOhm FDI_OVRVLTG R2519 1 2 100KOhm GND
FDI TERMINATION VOLTAGE OVERRIDE
- GPIO37 (FDI_OVRVLTG)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

+3VS R2520 1 2 200KOhm SATA_ODD_PRSNT#_R R2530 1 @ 2 10KOhm GND
DMI TERMINATION VOLTAGE OVERRIDE
- GPIO36 (SATA_ODD_PRSNT#)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

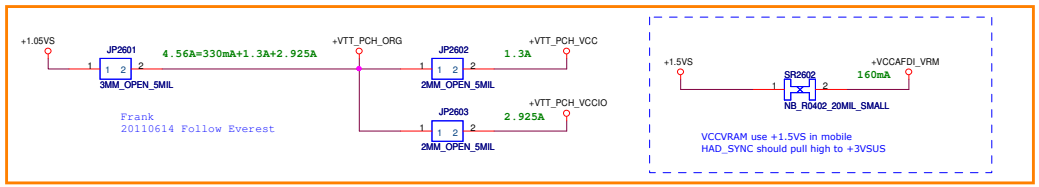
R1.1
add Zero Power ODD

WLAN_ON_R R2521 1 @ 2 1KOhm GND
PLL ON DIE VR ENABLE
HIGH - DISABLED (DEFAULT)
LOW - ENABLED

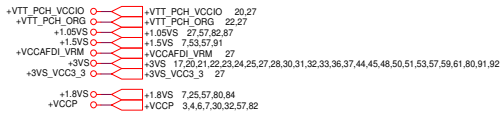
PEGATRON Title : PCH(6)_CPU,GPIO,MISC
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 25 of 93



R1.0

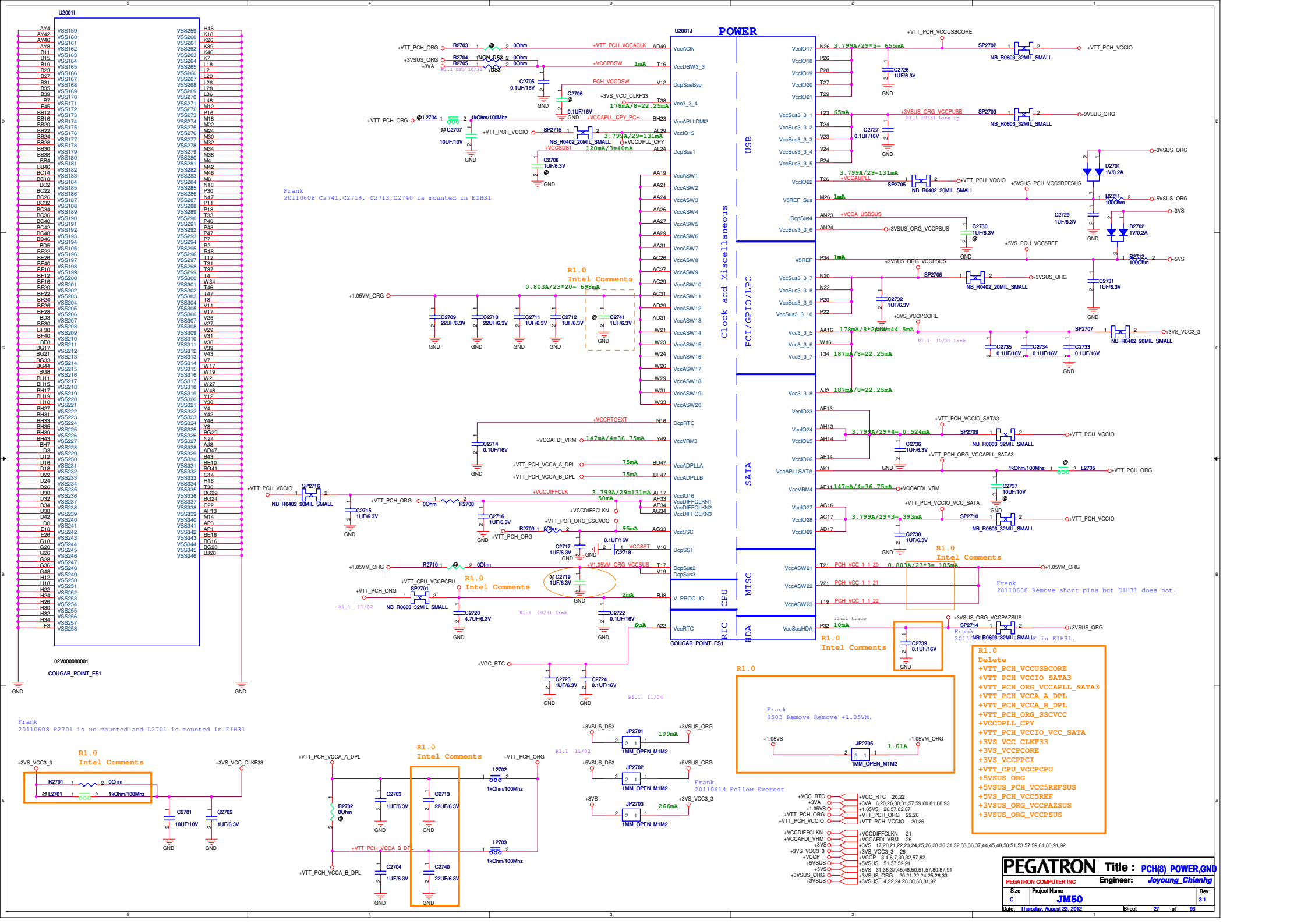


Frank
20110608 EVERST remove 1.8VS and +VTT_PCH_ORG



R1.0
Delete
+VTT_PCH_VCC
+VTT_PCH_VCCDPLL_EXP
+VTT_PCH_VCCAPLL_EXP
+VTT_PCH_VCCDPLL_FDI
+VTT_PCH_VCCAPLL_FDI
+3VS_VCCA3GBG
+3VS_VCC_GIO
+VCCA_DAC_1_2
+3VS_VCCA_LVDS
+3VM_VCCPSPI
+V_NVRAM_VCCPNAND
+1.8VS_VCCTX_LVD
+VCCIO_CPU_VCC_DMI
+VTT_PCH_ORG_VCCCLKDMI

PEGATRON	Title :	PCH(7)_POWER,GND	
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg	
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 26 of 93		


U2001I
COUGAR_POINT_ES1
02V000000001
U2001J
POWER
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
Frank
20110608 C2741,C2719, C2713,C2740 is mounted in EIH31
R1.0
Intel Comments
0.803A/23*20= 698mA
Frank
20110608 R2701 is un-mounted and L2701 is mounted in EIH31
Frank
0503 Remove Remove +1.05VM.
Frank
20110614 Follow Everest
Frank
20110608 Remove short pins but EIH31 does not.
R1.0
Delete
+VTT_PCH_VCCUSBCORE
+VTT_PCH_VCCIO_SATA3
+VTT_PCH_ORG_VCCAPLL_SATA3
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VTT_PCH_ORG_SSCVCC
+VCCDPLL_CPY
+VTT_PCH_VCCIO_VCC_SATA
+3VS_VCC_CLKF33
+3VS_VCCPCORE
+3VS_VCCPPCI
+VTT_CPU_VCCPCPU
+5VSUS_ORG
+5VSUS_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VSUS_ORG_VCCPAZSUS
+3VSUS_ORG_VCCPSUS
PEGATRON
Title : PCH(8)_POWER,GND
PEGATRON COMPUTER INC
Engineer: Joyoung_Chianhg
Size C
Project Name JM50
Rev 3.1
Date: Thursday, August 23, 2012
Sheet 27 of 93

PCH SPI ROM

SHARE ROM CONFIG1

U2801	@	
U2802	@	
U2803	ME+BIOS+EC	4MB

ummount:
R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802,R2869, R2870, R2868, D2802, U2801

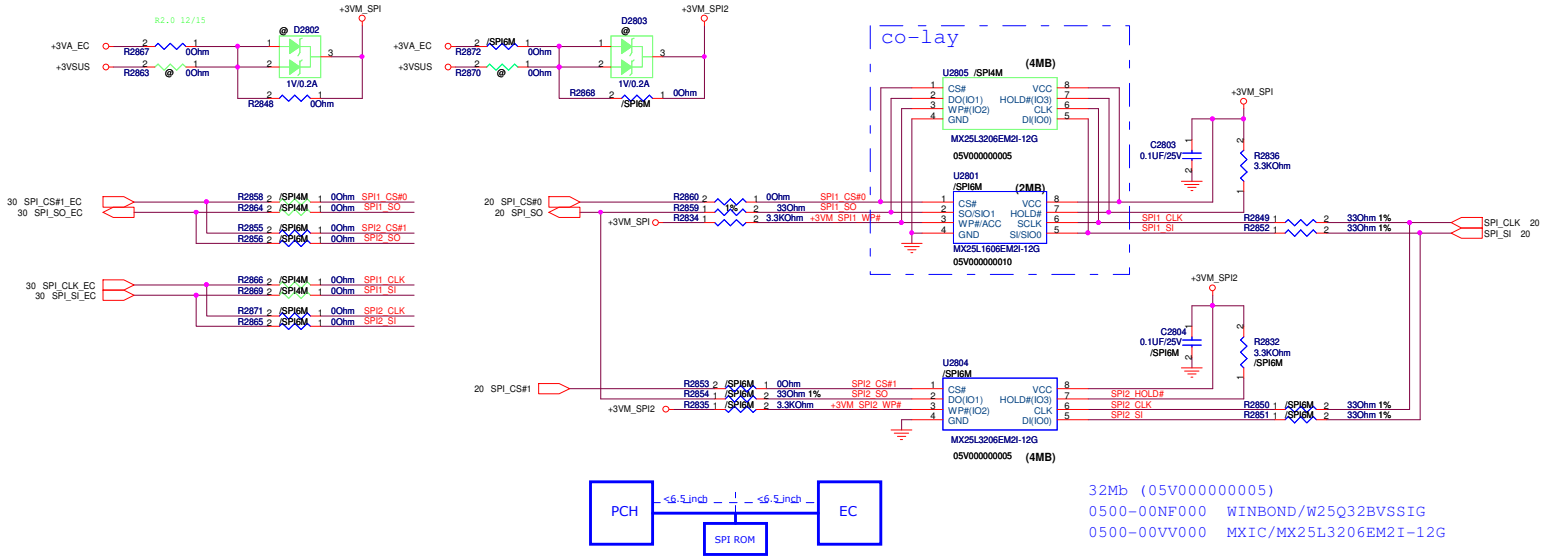
SHARE ROM CONFIG2

U2801	ME Firmware	2MB
U2802	EC+BIOS	4MB

ummount:
R2858, R2862, R2866, R2867, U2803

PCH SPI ROM

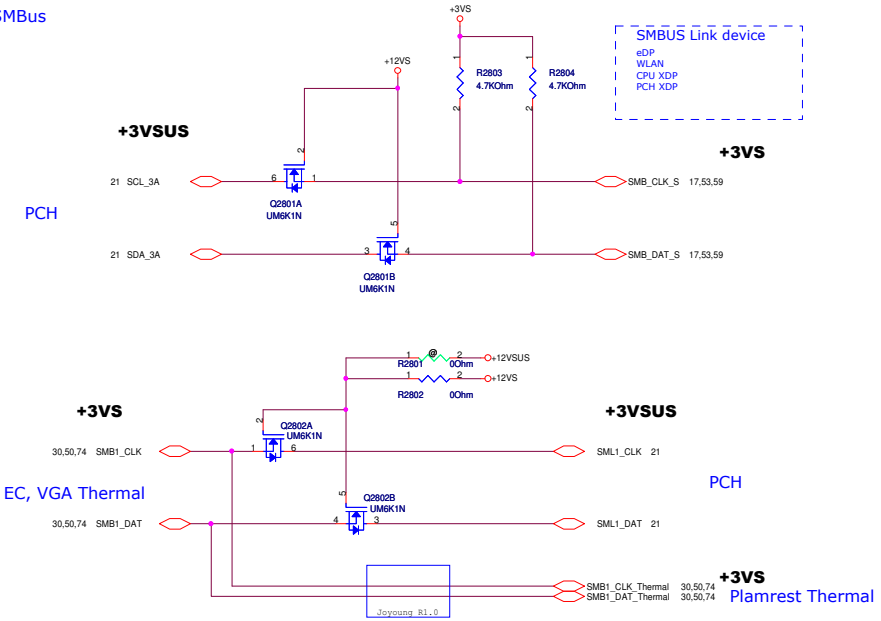
+3VA_EC reserved for share ROM



SPI Debug Connector

layout space issue, so remove J2801.

PCH SMBus



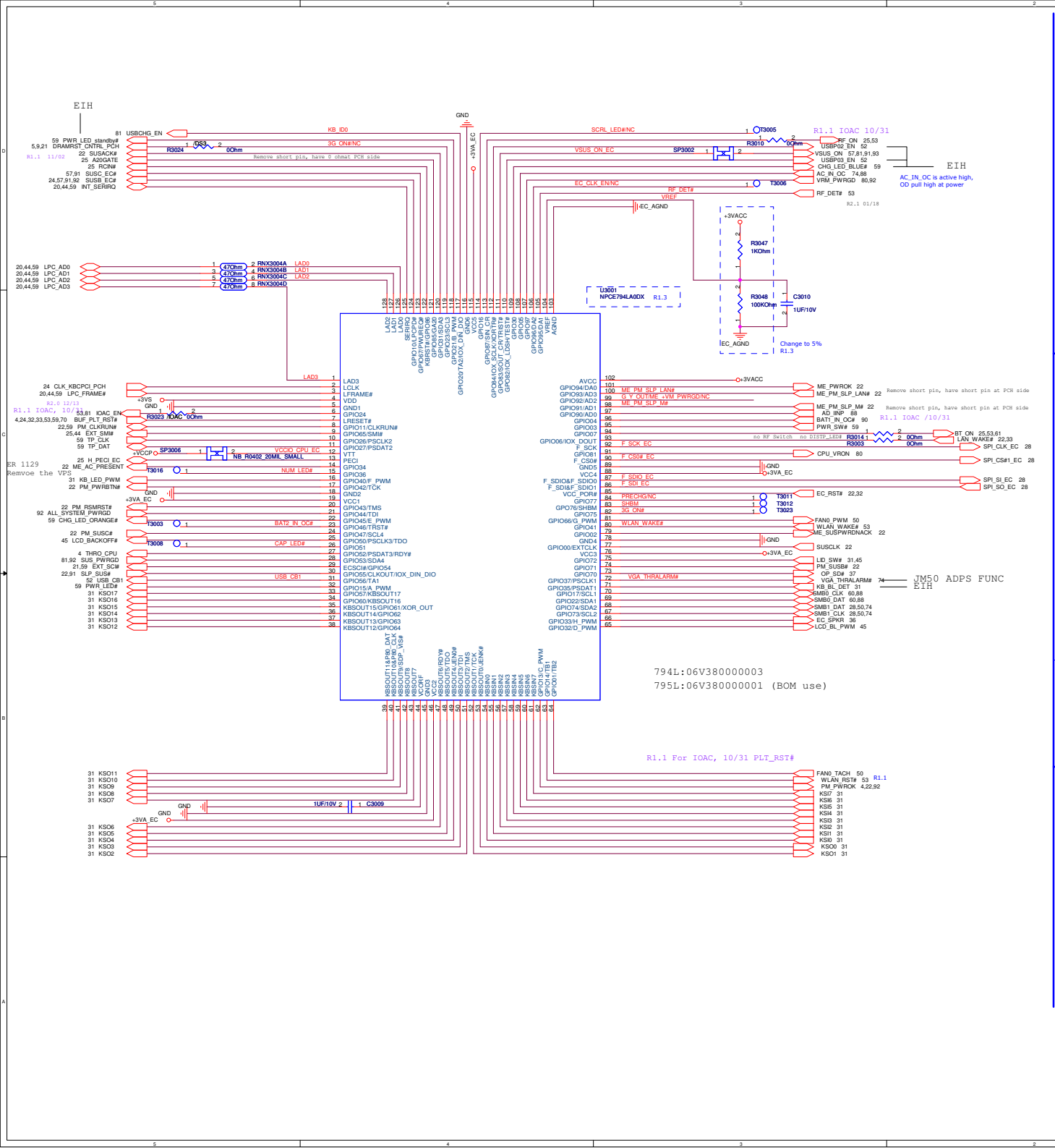
PEGATRON Title : PCH(9)_SPI,SMB
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 28 of 93

PEGATRON Title : CLK_ICS9LRS3197

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	JM50	3.1

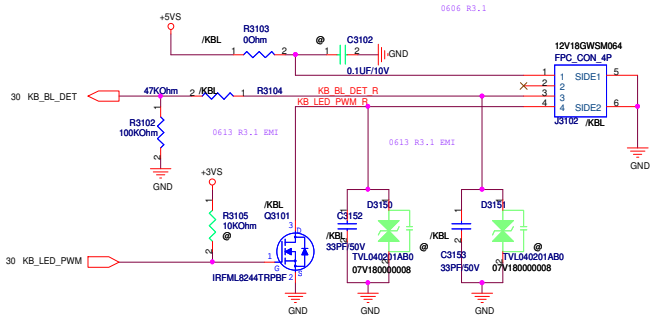
Date: Thursday, August 23, 2012 Sheet 29 of 93



PEGATRON	Title : NPCE794L		
	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 1.3
Date: Thursday, August 23, 2012	Sheet 30 of 93		

KB backlight

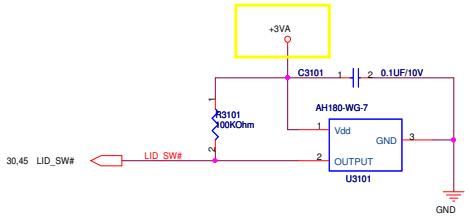
R3.1 Add 4P CON for KB Backlight Kevin 0601



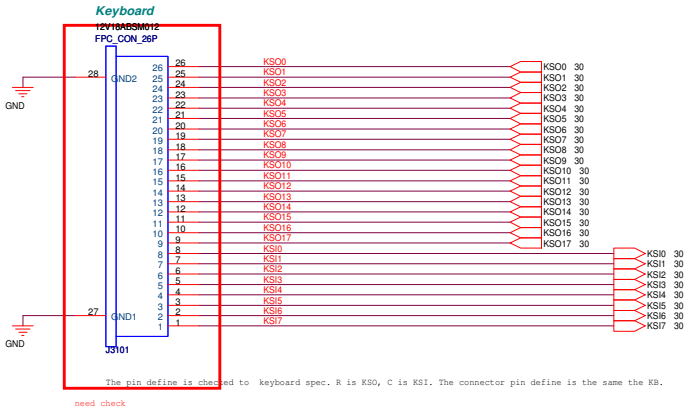
LID Switch

SR-85

R1.0 change net name. Joyoung 0630

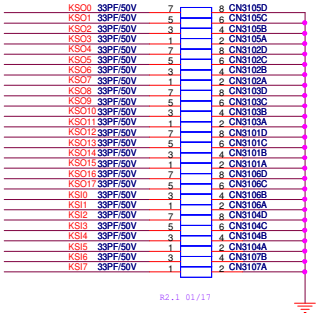


Keyboard



The pin define is checked to keyboard spec. R is KSO, C is KSI. The connector pin define is the same the KB.

need check



R2.1 01/17

PEGATRON Title : EC_IT8512(2)KB, TP,FP

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 31 of 93

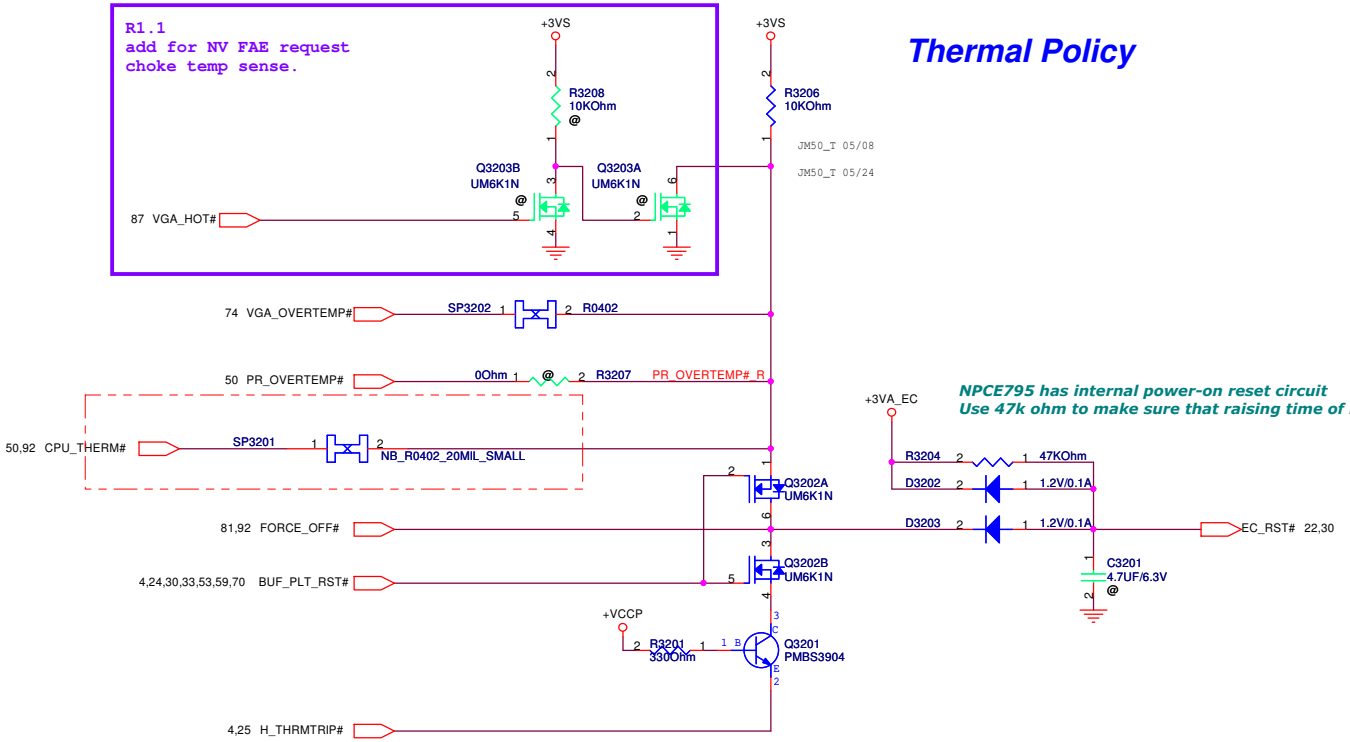
+VCCP +VCCP 3,4,6,7,30,57,82

+3VA_EC +3VA_EC 28,30

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

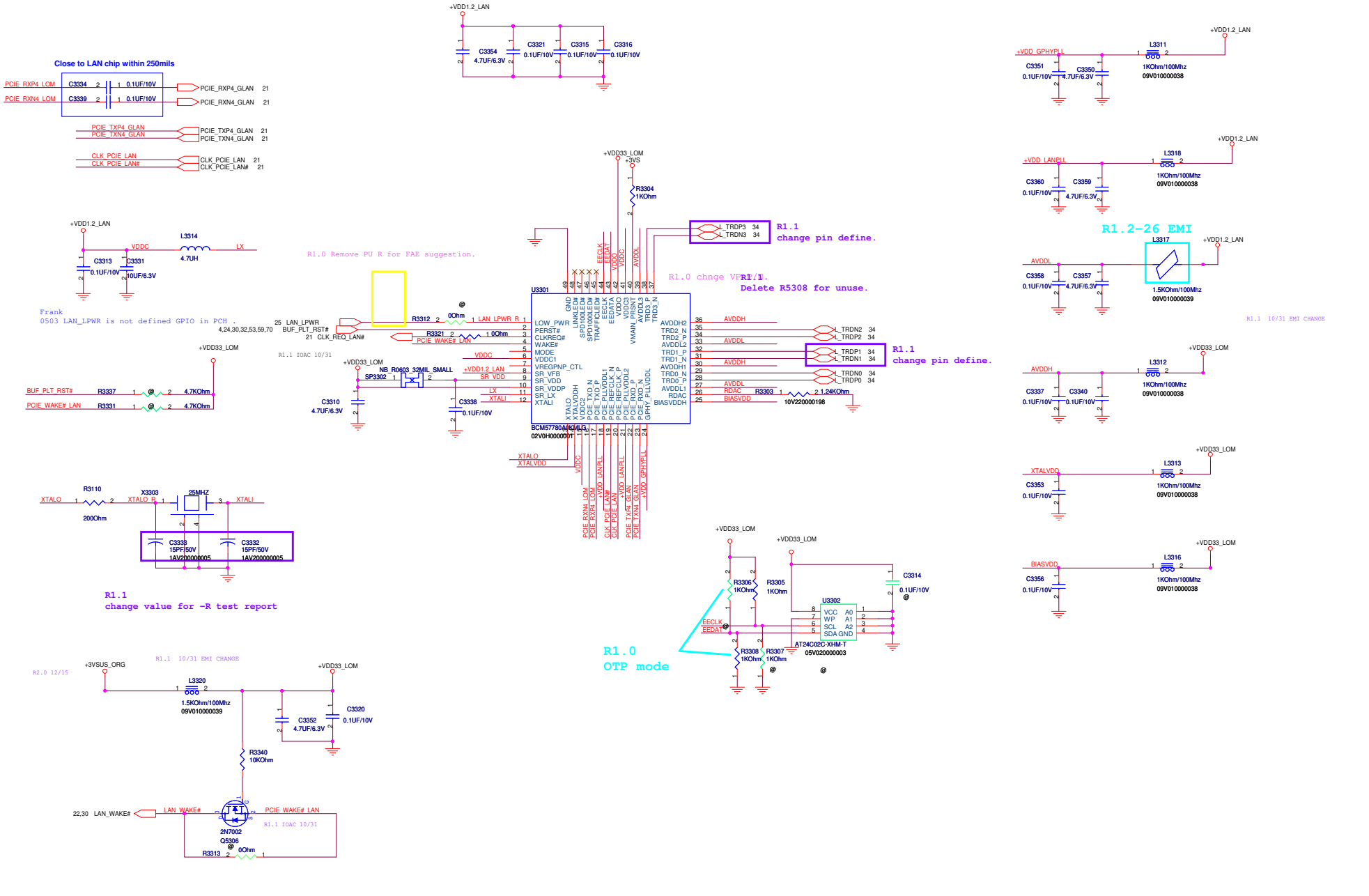
R1.1
add for NV FAE request
choke temp sense.

Thermal Policy



NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us

PEGATRON	Title : RST_Reset Circuit		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 32 of 93		



PEGATRON	Title : LAN_BCM57780		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50	Rev: 3.1	
Date: Thursday, August 23, 2012	Sheet 33 of 93		

Joyoung R1.0
FAE suggest common mode choke is on chip side.

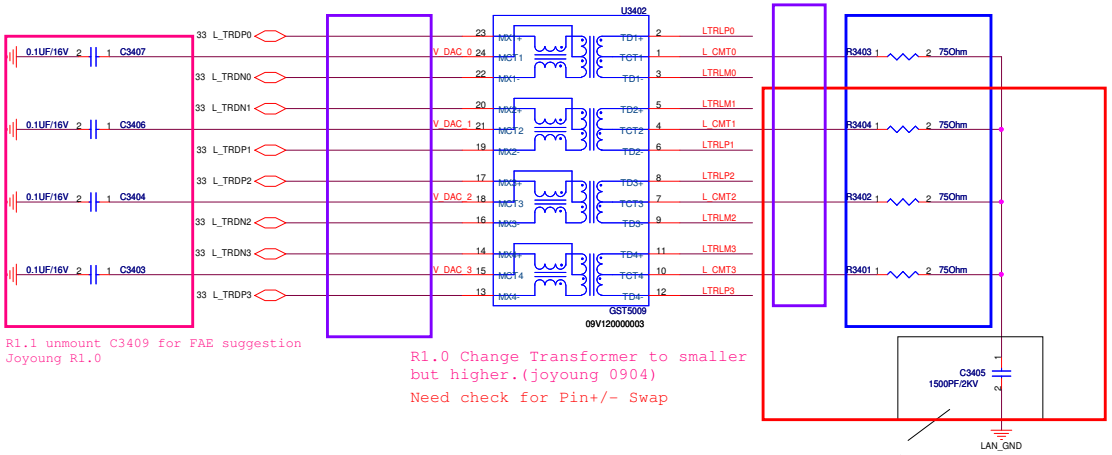
R1.1 Add 0 OHM for FAE suggestion 0809
JM50: FAE suggest remove

R1.1 Swap L_TRDP3 L_TRDN3 & L_TRDP1 L_TRDN1

R1.1 remove CAP of V_DAC_3, V_DAC_2 and V_DAC_1 for FAE suggestion

R1.1 Remove R3405~R3407 & C3409

R1.1 Mount R3401~R3403 for FAE suggestion 0809



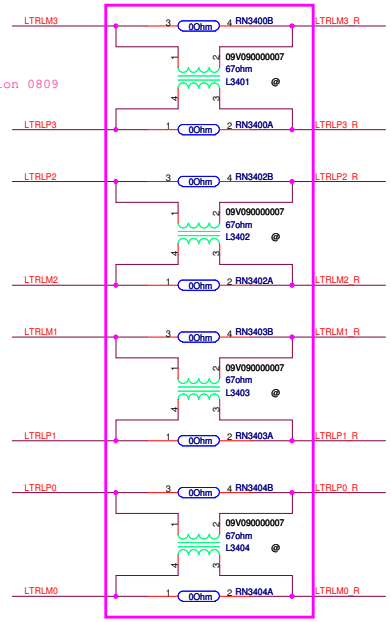
R1.1 unmount C3409 for FAE suggestion
Joyoung R1.0

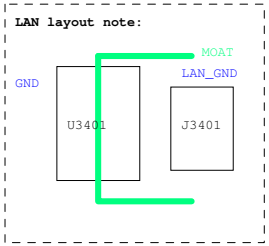
R1.0 Change Transformer to smaller but higher.(joyoung 0904)

Need check for Pin+/- Swap

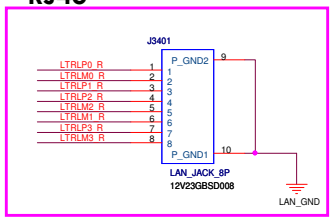
PR_S12

Co-lay C3409 & C3411
Co-lay C3410 & C3412



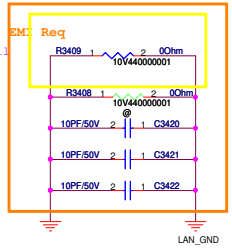


RJ45



Change RJ45 CON3401

R1.1 EMI Request 4.7PF & Set Close to Connector, then removed all



R1.0 Reserve D3401 for EMI.

R1.0 Mount R3408 for FAE suggestion

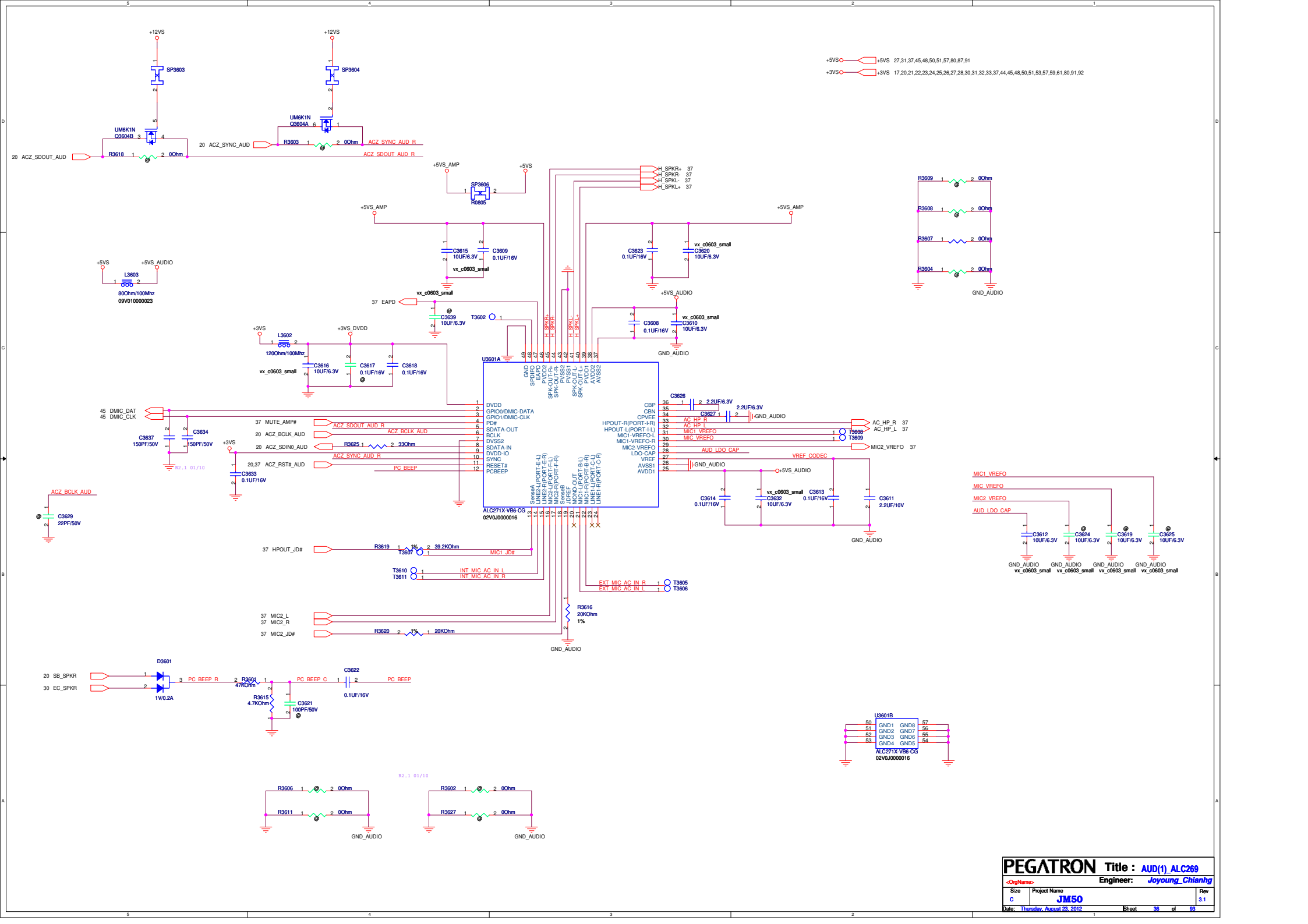
PEGATRON	Title : RJ45	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 34 of 93	

PEGATRON Title : MDC CONN

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 35 of 93


+5VS 27,31,37,45,48,50,51,57,80,87,91
+3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,37,44,45,48,50,51,53,57,59,61,80,91,92
SP3603
SP3604
SP3606
R0805
UM6K1N
Q3604B
Q3604A
R3618 0Ohm
R3603 0Ohm
20 ACZ_SDOUT_AUD
20 ACZ_SYNC_AUD
ACZ_SYNC_AUD_R
ACZ_SDOUT_AUD_R
+5VS_AMP
+5VS
+5VS_AUDIO
+3VS
+3VS_DVDD
L3603
80Ohm/100Mhz
09V010000023
L3602
120Ohm/100Mhz
C3615 10UF/6.3V
C3609 0.1UF/16V
C3623 0.1UF/16V
C3620 10UF/6.3V
C3608 0.1UF/16V
C3610 10UF/6.3V
C3639 10UF/6.3V
C3616 10UF/6.3V
C3617 0.1UF/16V
C3618 0.1UF/16V
vx_c0603_small
37 EAPD
T3602
H_SPKR+ 37
H_SPKR- 37
H_SPKL- 37
H_SPKL+ 37
R3609 0Ohm
R3608 0Ohm
R3607 0Ohm
R3604 0Ohm
GND_AUDIO
U3601A
ALC271X-VB6-CG
02V0J0000016
DVDD
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PD#
SDATA-OUT
BCLK
DVSS2
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
CBP
CBN
CPVEE
HPOUT-R(PORT-I-R)
HPOUT-L(PORT-I-L)
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
LDO-CAP
VREF
AVSS1
AVDD1
C3626 2.2UF/6.3V
C3627 2.2UF/6.3V
AC_HP_R 37
AC_HP_L 37
MIC1_VREFO
MIC_VREFO
MIC2_VREFO 37
AUD_LDO_CAP
VREF_CODEC
C3614 0.1UF/16V
C3632 10UF/6.3V
C3613 0.1UF/16V
C3611 2.2UF/10V
45 DMIC_DAT
45 DMIC_CLK
37 MUTE_AMP#
20 ACZ_BCLK_AUD
20 ACZ_SDIN0_AUD
20,37 ACZ_RST#_AUD
PC_BEEP
R3625 33Ohm
C3637 150PF/50V
C3634 150PF/50V
C3633 0.1UF/16V
C3629 22PF/50V
R2.1 01/10
37 HPOUT_JD#
R3619 39.2KOhm 1%
T3607
MIC1_JD#
T3610
T3611
INT_MIC_AC_IN_L
INT_MIC_AC_IN_R
EXT_MIC_AC_IN_R
EXT_MIC_AC_IN_L
T3605
T3606
R3616 20KOhm 1%
37 MIC2_L
37 MIC2_R
37 MIC2_JD#
R3620 20KOhm 1%
MIC1_VREFO
MIC_VREFO
MIC2_VREFO
AUD_LDO_CAP
C3612 10UF/6.3V
C3624 10UF/6.3V
C3619 10UF/6.3V
C3625 10UF/6.3V
vx_c0603_small
D3601
1V/0.2A
20 SB_SPKR
30 EC_SPKR
PC_BEEP_R
PC_BEEP_C
R3601 47KOhm
R3615 4.7KOhm
C3621 100PF/50V
C3622 0.1UF/16V
U3601B
ALC271X-VB6-CG
02V0J0000016
R3606 0Ohm
R3611 0Ohm
R3602 0Ohm
R3627 0Ohm
PEGATRON
Title : AUD(1)_ALC269
<OrgName>
Engineer: Joyoung_Chianhg
Size C
Project Name JM50
Rev 3.1
Date: Thursday, August 23, 2012
Sheet 36 of 93

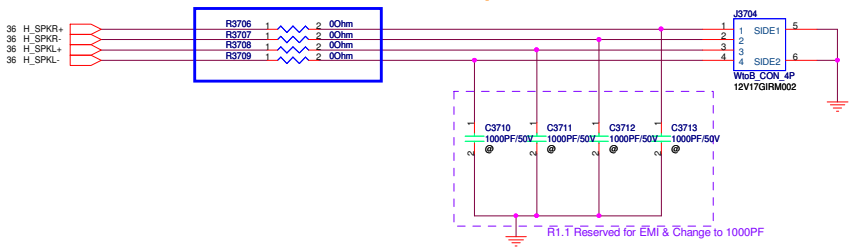
+5VS +5VS 27,31,36,45,48,50,51,57,80,87,91

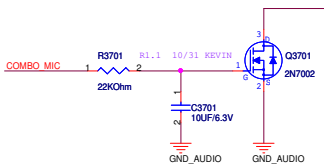
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,44,45,48,50,51,53,57,59,61,80,91,92

+5VS_AUDIO +5VS_AUDIO 36

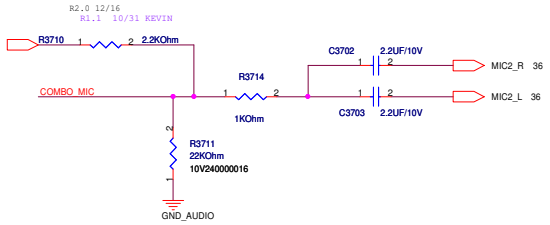
Internal Speaker Conn.

add R3706, R3707, R3708, R3709 for EMI request



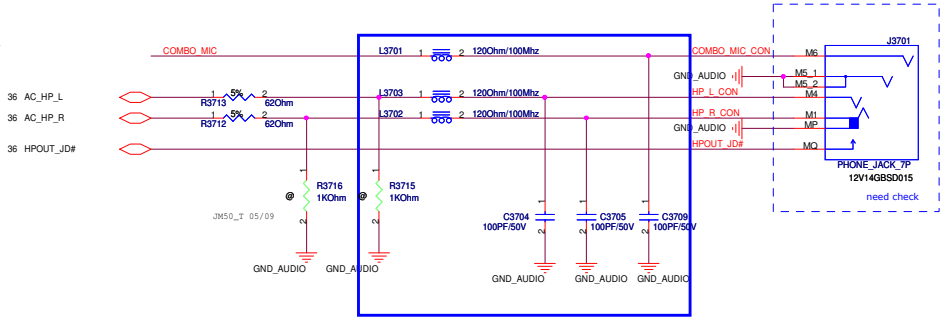


Need change 0702-0028000 in next stage

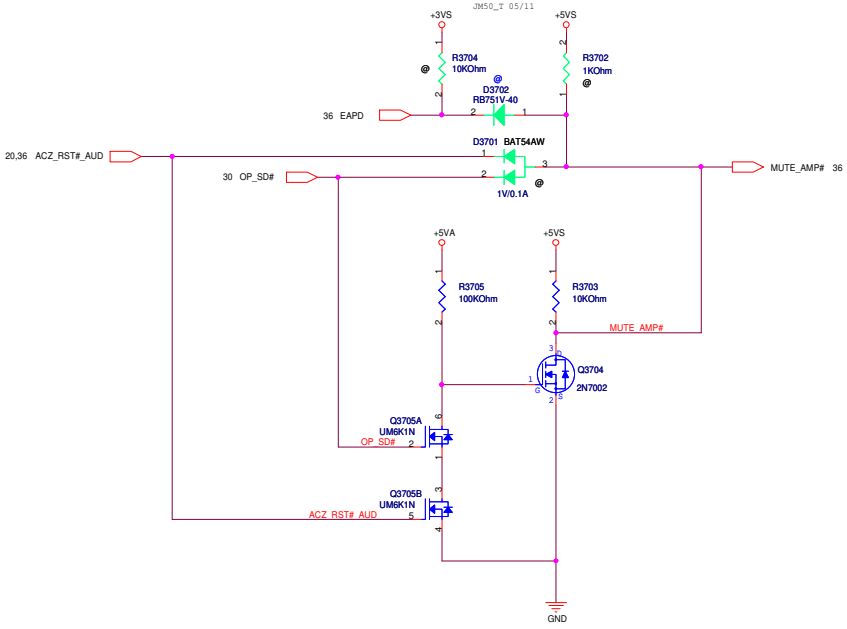


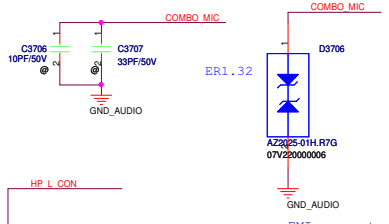
add R3722, R3723 and C3723, C3725 change 100pFfor EMI request

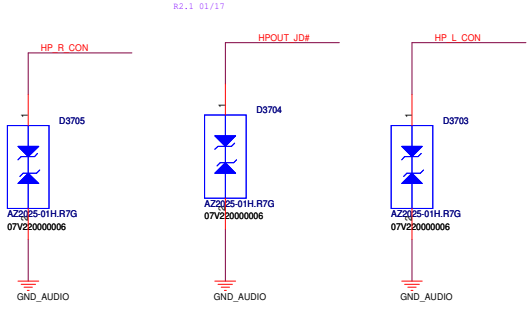
ER1.11

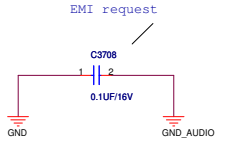


Close J6701









PEGATRON	Title :	AUD(2)_AMP,JACK
<OrgName>	Engineer:	Joyoung_Chianhg
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 37 of 93	

PEGATRON Title : AUD(3)_FM2010

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 38 of 93

PEGATRON

Title : AUD(4)_****

<OrgName>

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 39 of 93

PEGATRON Title : TPM_****

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 40 of 93

PEGATRON Title : CB(2)_R5C833

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 41 of 93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+12V +12V 60,91

PEGATRON Title : CB(3)_4in1 CardReader

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 42 of 93

PEGATRON Title : CB(4)_NewCard

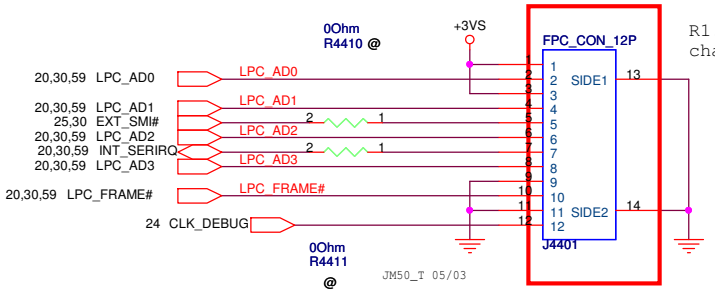
<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 43 of 93

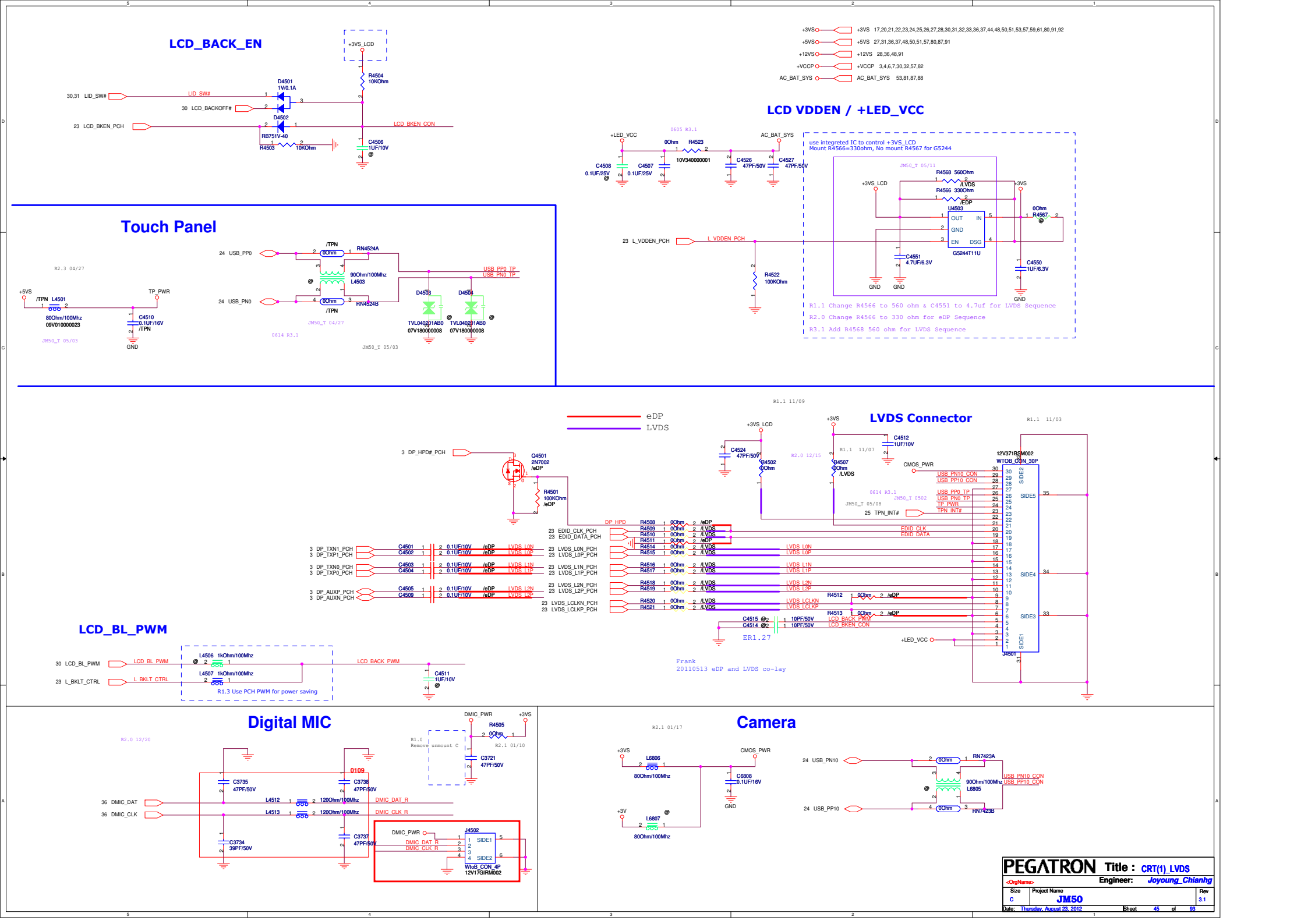
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,45,48,50,51,53,57,59,61,80,91,92

LPC Debug Port



R1.1
change pin define to IEIE cable.

PEGATRON	Title : BUG_Debug	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: B	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 44 of 93	


LCD_BACK_EN
+3VS_LCD
R4504 10KOhm
30,31 LID_SW#
LID_SW#
D4501 1V/0.1A
30 LCD_BACKOFF#
D4502
23 LCD_BKEN_PCH
LCD_BKEN_CON
RB751V-40
R4503
10KOhm
C4506 1UF/10V
+3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,48,50,51,53,57,59,61,80,91,92
+5VS 27,31,36,37,48,50,51,57,80,87,91
+12VS 28,36,48,91
+VCCP 3,4,6,7,30,32,57,82
AC_BAT_SYS 53,81,87,88
LCD VDDEN / +LED_VCC
+LED_VCC
0605 R3.1
0Ohm R4523
AC_BAT_SYS
10V340000001
C4508 0.1UF/25V
C4507 0.1UF/25V
C4526 47PF/50V
C4527 47PF/50V
use integreted IC to control +3VS_LCD
Mount R4566=330ohm, No mount R4567 for G5244
JM50_T 05/11
R4568 560Ohm /LVDS
R4566 330Ohm /EDP
+3VS_LCD
+3VS
U4503
OUT IN
GND
EN DSG
G5244T11U
0Ohm R4567
C4551 4.7UF/6.3V
C4550 1UF/6.3V
GND
23 L_VDDEN_PCH
L_VDDEN_PCH
R4522 100KOhm
R1.1 Change R4566 to 560 ohm & C4551 to 4.7uf for LVDS Sequence
R2.0 Change R4566 to 330 ohm for eDP Sequence
R3.1 Add R4568 560 ohm for LVDS Sequence
Touch Panel
R2.3 04/27
+5VS
/TPN L4501
TP_PWR
80Ohm/100Mhz
09V010000023
C4510 0.1UF/16V /TPN
GND
JM50_T 05/03
24 USB_PP0
24 USB_PN0
/TPN
0Ohm
RN4524A
90Ohm/100Mhz
L4503
RN4524B
USB_PP0_TP
USB_PN0_TP
D4503
D4504
TVL040201AB0
07V180000008
JM50_T 04/27
0614 R3.1
JM50_T 05/03
LCD_BL_PWM
30 LCD_BL_PWM
LCD_BL_PWM
L4506 1kOhm/100Mhz
23 L_BKLT_CTRL
L_BKLT_CTRL
L4507 1kOhm/100Mhz
LCD_BACK_PWM
C4511 1UF/10V
R1.3 Use PCH PWM for power saving
R1.1 11/09
eDP
LVDS
LVDS Connector
R1.1 11/03
3 DP_HPD#_PCH
Q4501 2N7002 /eDP
R4501 100KOhm /eDP
DP_HPD
23 EDID_CLK_PCH
23 EDID_DATA_PCH
3 DP_TXN1_PCH
3 DP_TXP1_PCH
3 DP_TXN0_PCH
3 DP_TXP0_PCH
3 DP_AUXP_PCH
3 DP_AUXN_PCH
C4501 0.1UF/10V /eDP LVDS_L0N
C4502 0.1UF/10V /eDP LVDS_L0P
C4503 0.1UF/10V /eDP LVDS_L1N
C4504 0.1UF/10V /eDP LVDS_L1P
C4505 0.1UF/10V /eDP LVDS_L2N
C4509 0.1UF/10V /eDP LVDS_L2P
23 LVDS_L0N_PCH
23 LVDS_L0P_PCH
23 LVDS_L1N_PCH
23 LVDS_L1P_PCH
23 LVDS_L2N_PCH
23 LVDS_L2P_PCH
23 LVDS_LCLKN_PCH
23 LVDS_LCLKP_PCH
R4508 0Ohm /eDP
R4509 0Ohm /LVDS
R4510 0Ohm /LVDS
R4511 0Ohm /eDP
R4514 0Ohm /LVDS
R4515 0Ohm /LVDS
R4516 0Ohm /LVDS
R4517 0Ohm /LVDS
R4518 0Ohm /LVDS
R4519 0Ohm /LVDS
R4520 0Ohm /LVDS
R4521 0Ohm /LVDS
LVDS_L0N
LVDS_L0P
LVDS_L1N
LVDS_L1P
LVDS_L2N
LVDS_L2P
LVDS_LCLKN
LVDS_LCLKP
R2.0 12/15
+3VS_LCD
C4524 47PF/50V
R4502 0Ohm
+3VS
R1.1 11/07
C4512 1UF/10V
R4507 0Ohm /LVDS
CMOS_PWR
0614 R3.1
JM50_T 05/08
JM50_T 0502
25 TPN_INT#
TPN_INT#
EDID_CLK
EDID_DATA
R4512 0Ohm /eDP
R4513 0Ohm /eDP
C4515 @ 10PF/50V
C4514 @ 10PF/50V
LCD_BACK_PWM
LCD_BKEN_CON
ER1.27
+LED_VCC
12V371BSM002
WTOB_CON_30P
USB_PN10_CON
USB_PP10_CON
USB_PP0_TP
USB_PN0_TP
TP_PWR
SIDE1
SIDE2
SIDE3
SIDE4
SIDE5
J4501
Frank
20110513 eDP and LVDS co-lay
Digital MIC
R2.0 12/20
DMIC_PWR
+3VS
R4505 0Ohm
R1.0 Remove unmount C
R2.1 01/10
C3721 47PF/50V
0109
C3735 47PF/50V
C3738 47PF/50V
36 DMIC_DAT
36 DMIC_CLK
L4512 120Ohm/100Mhz
L4513 120Ohm/100Mhz
DMIC_DAT_R
DMIC_CLK_R
C3734 39PF/50V
C3737 47PF/50V
J4502
SIDE1
SIDE2
WtoB_CON_4P
12V17GIRM002
Camera
R2.1 01/17
+3VS
L6806 80Ohm/100Mhz
+3V
L6807 80Ohm/100Mhz
CMOS_PWR
C6808 0.1UF/16V
GND
24 USB_PN10
24 USB_PP10
RN7423A
90Ohm/100Mhz
L6805
RN7423B
USB_PN10_CON
USB_PP10_CON
PEGATRON
Title : CRT(1)_LVDS
<OrgName>
Engineer: Joyoung_Chianhg
Size C
Project Name JM50
Rev 3.1
Date: Thursday, August 23, 2012
Sheet 45 of 93

PEGATRON Title : CRT

BU1-RD Div.1-HW RD Dept.1 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	JM50	3.1

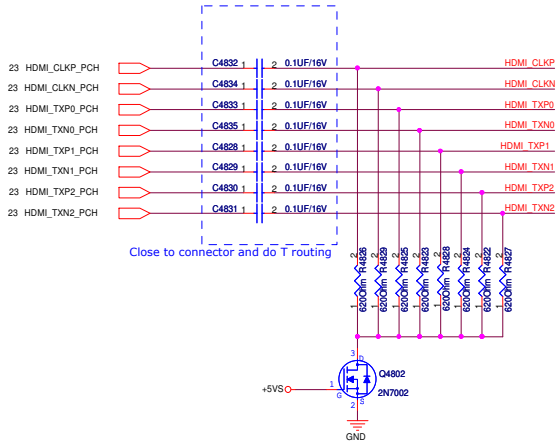
Date: Thursday, August 23, 2012 Sheet 46 of 93

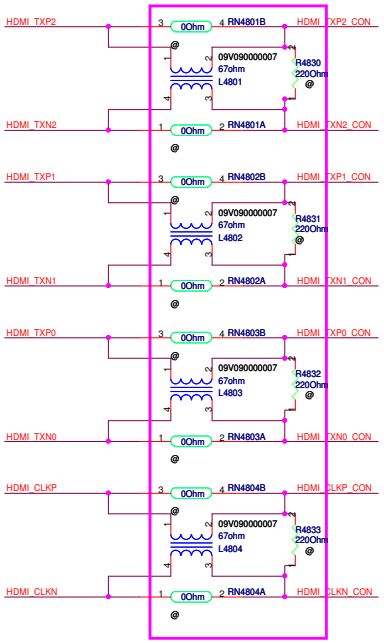
PEGATRON Title : CRT(3)_Display Port

<OrgName> Engineer: Joyoung_Chianhg

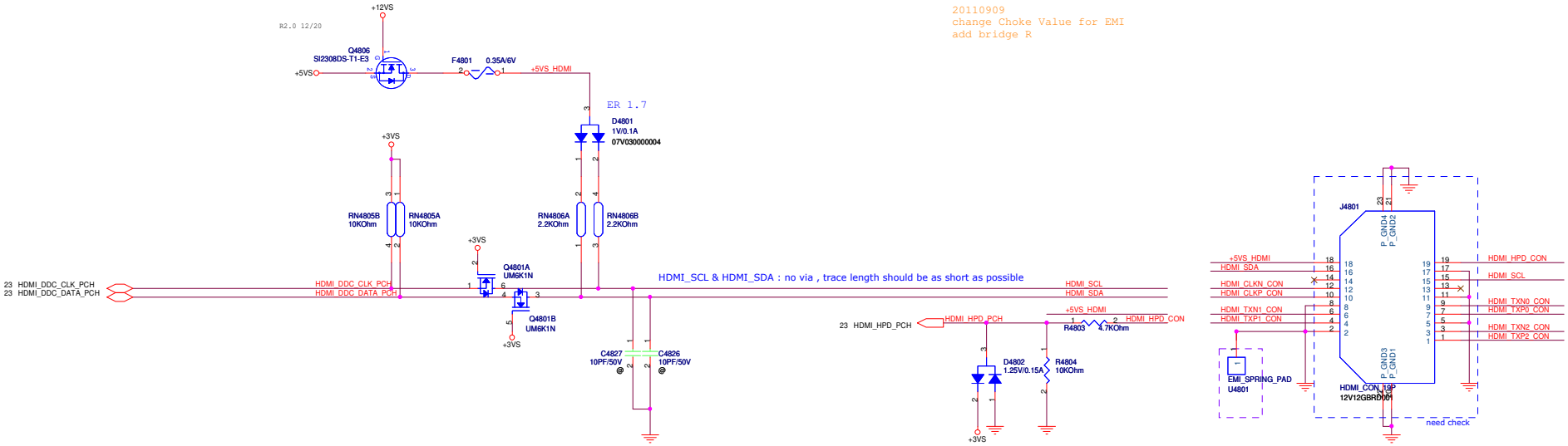
Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 47 of 93





20110909
change Choke Value for EMI
add bridge R



R1.1 EMI Request for Spring PAD(close to HDMI conn)

+12VS +12VS 28,36,91

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,50,51,53,57,59,61,80,91,92

+5VS +5VS 27,31,36,37,45,50,51,57,80,87,91

PEGATRON Title : TV(1)_HDMI

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 48 of 93

PEGATRON Title : TV(2)_****

<OrgName> Engineer: Joyoung_Chianhg

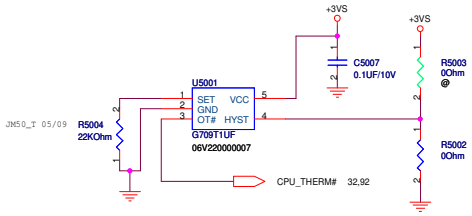
Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 49 of 93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,51,53,57,59,61,80,91,92

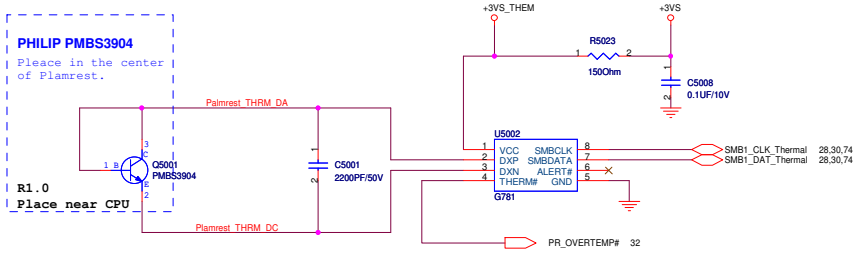
+5VS +5VS 27,31,36,37,45,48,51,57,80,87,91

CPU Thermal Sensor



(10°C for HYST =VCC)
(2°C for HYST = GND)
Hysteresis prevents the output from oscillating when the temperature is near the trip point.

DIMM Thermal Sensor

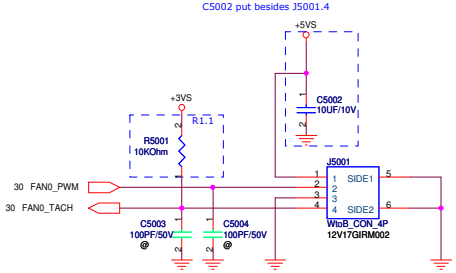


U5002 place neer power, CPU, PCH area,

SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan

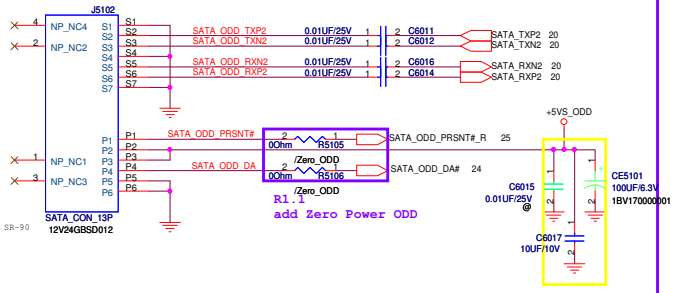


PEGATRON	Title : FAN_Fan,Sensor	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 50 of 93	

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,53,57,59,61,80,91,92

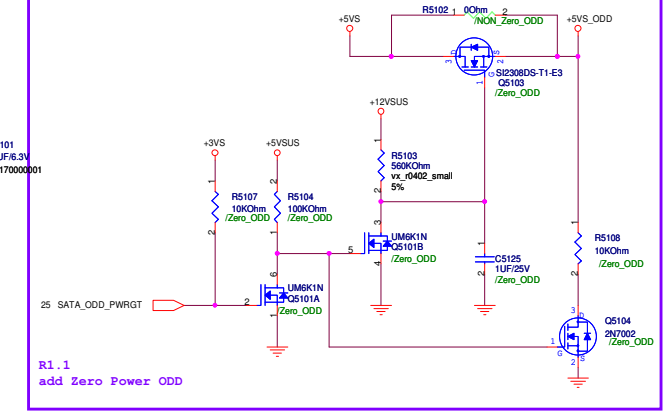
+5VS +5VS 27,31,36,37,45,48,50,57,80,87,91

ODD

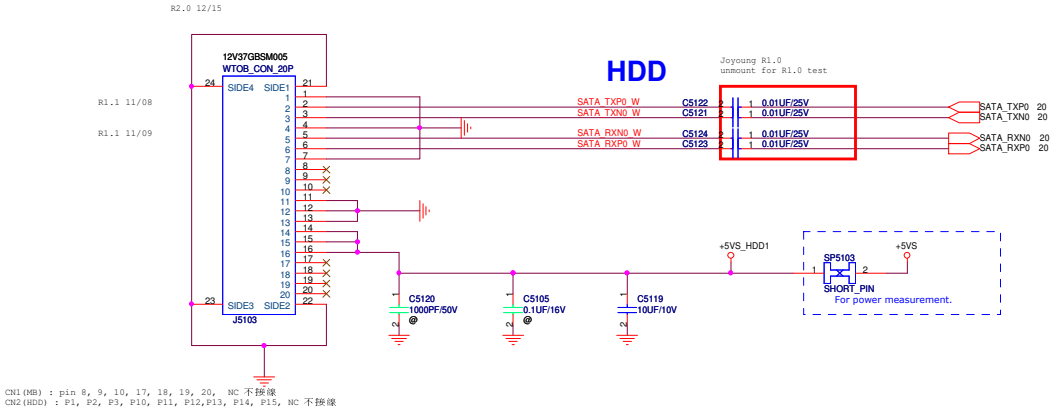


ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



Connector for Cable



CN1(MB) : pin 8, 9, 10, 17, 18, 19, 20, NC 不接線
CN2(HDD) : P1, P2, P3, P10, P11, P12,P13, P14, P15, NC 不接線

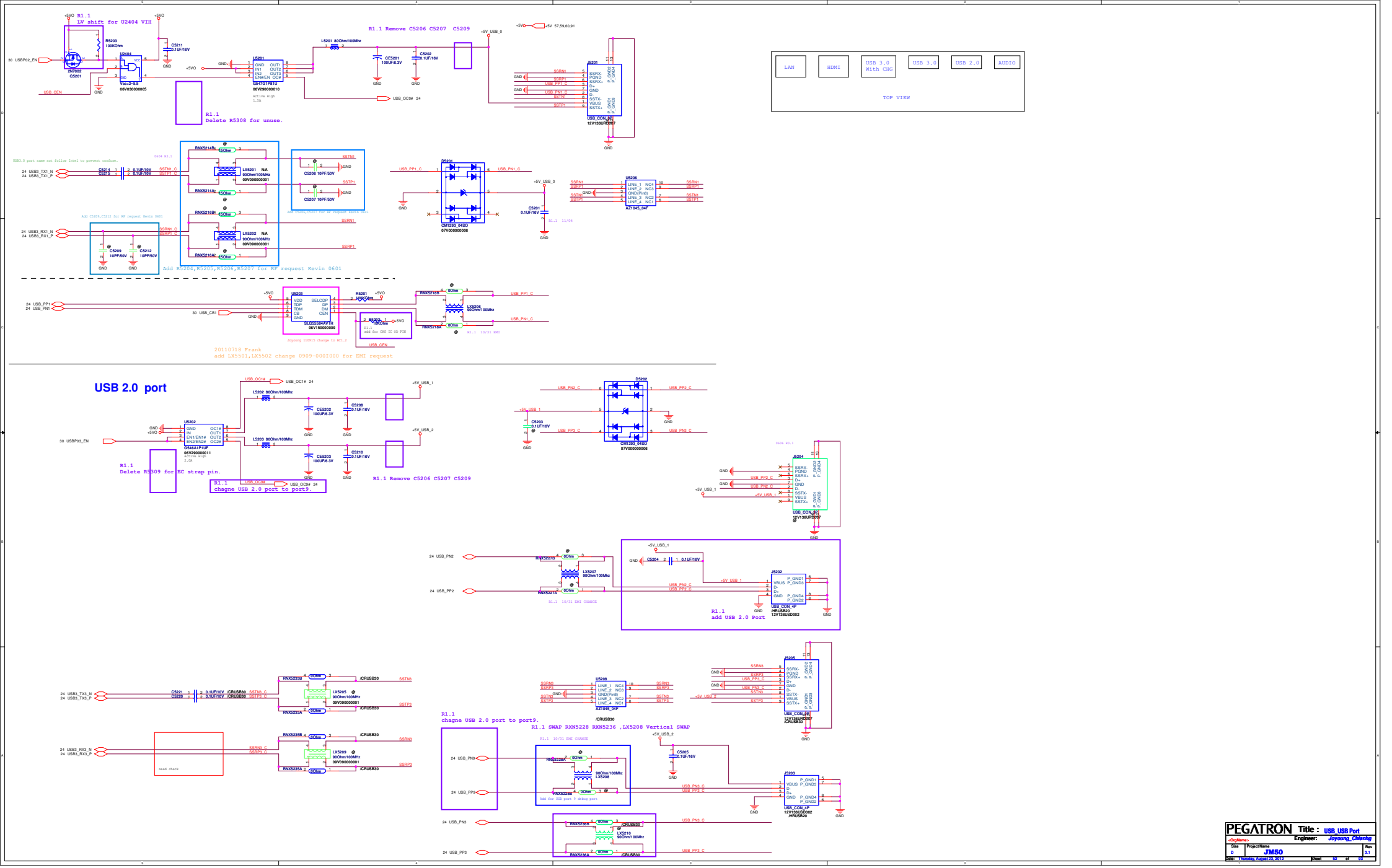
R1.1 11/02 Remove HDD SATA CONN PART

PEGATRON Title : XDD_HDD,ODD

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 51 of 93



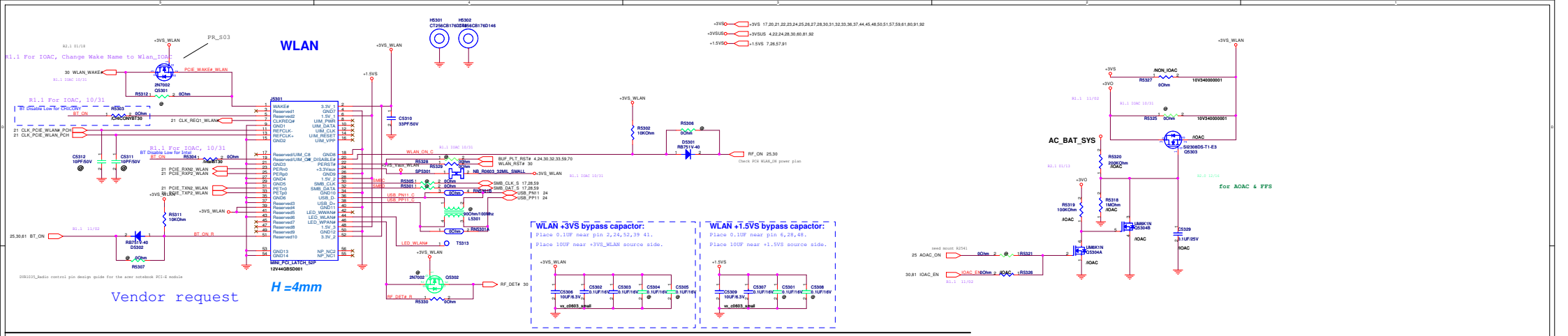
PEGATRON Title : USB_USB Port

Engineer: Joyoung_Chiang

Size	Project Name	Rev
D	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 52 of 93

WLAN



WLAN +3VS bypass capactor:

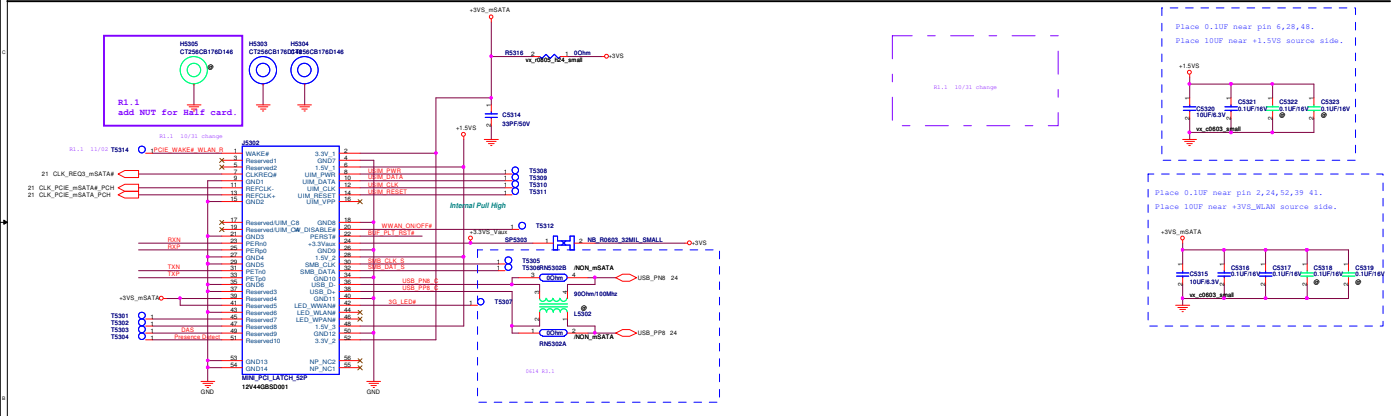
Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VS_WLAN source side.

WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.



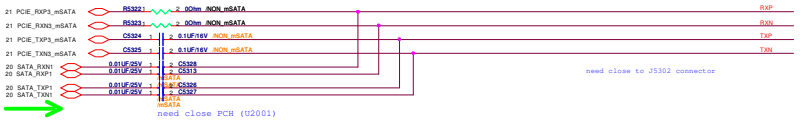
Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VS_WLAN source side.

PCIe & mSATA co-lay



PEGATRON Title : USB3.0

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 54 of 93

PEGATRON Title : Fersco USB 3.0

BG1-CSC-HW R&D Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
A2	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 55 of 93

+3VA +3VA 6,20,26,27,30,31,57,59,60,81,88,93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+5VSUS +5VSUS 51,57,59,91

+5VA +5VA 37,60,81,91

+5V +5V 57,59,60,91

+5VS +5VS 27,31,36,37,45,48,50,51,57,80,87,91

AC_BAT_SYS AC_BAT_SYS 45,53,81,87,88

+3V +3V 24,45,57,59,61,91

30,59 PWR_LED#

30,59 PWR_LED_standby#

30,59 CHG_LED_BLUE#

30,59 CHG_LED_ORANGE#

PEGATRON Title : LED_Indicator

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 56 of 93

+3VA +3VA 6,20,26,27,30,31,59,60,81,88,93

+VCORE +VCORE 6,9,11,80

+VGFX_CORE +VGFX_CORE 7,9,80

+VCCP +VCCP 3,4,6,7,30,32,82

+0.75VS +0.75VS 16,17,83

+1.05VS +1.05VS 26,27,82,87

+1.5VS +1.5VS 7,26,53,91

+1.8VS +1.8VS 7,25,26,80,84

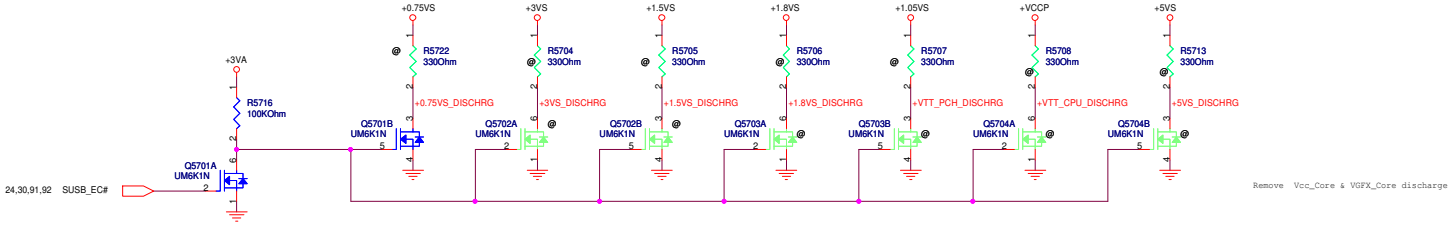
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,59,61,80,91,92

+5VS +5VS 27,31,36,37,45,48,50,51,80,87,91

+1.5V +1.5V 5,16,17,18,60,83

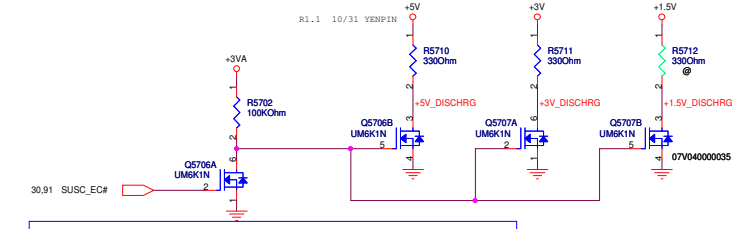
+3V +3V 24,45,59,61,91

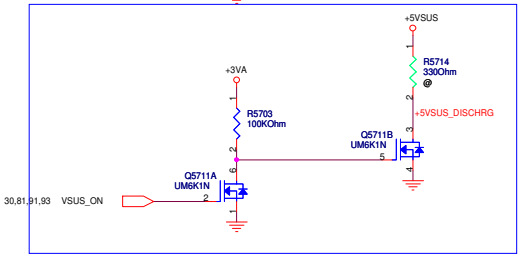
+5V +5V 59,60,91

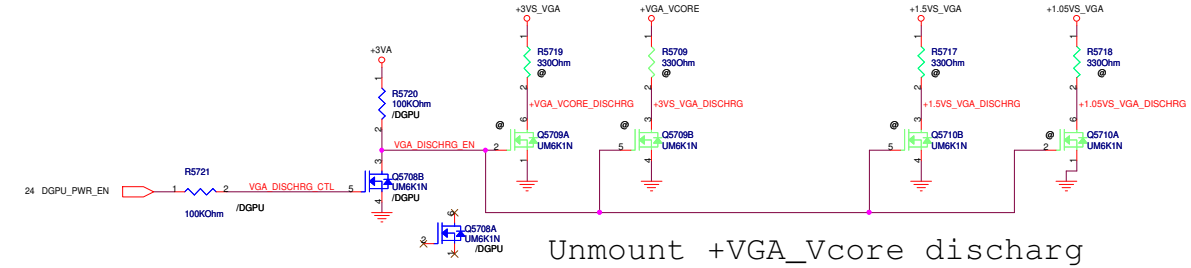


Remove Vcc_Core & VGFX_Core discharge

R1.1 10/31 YENPIN







Unmount +VGA_Vcore discharg

PEGATRON Title : DSG_Discharge

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

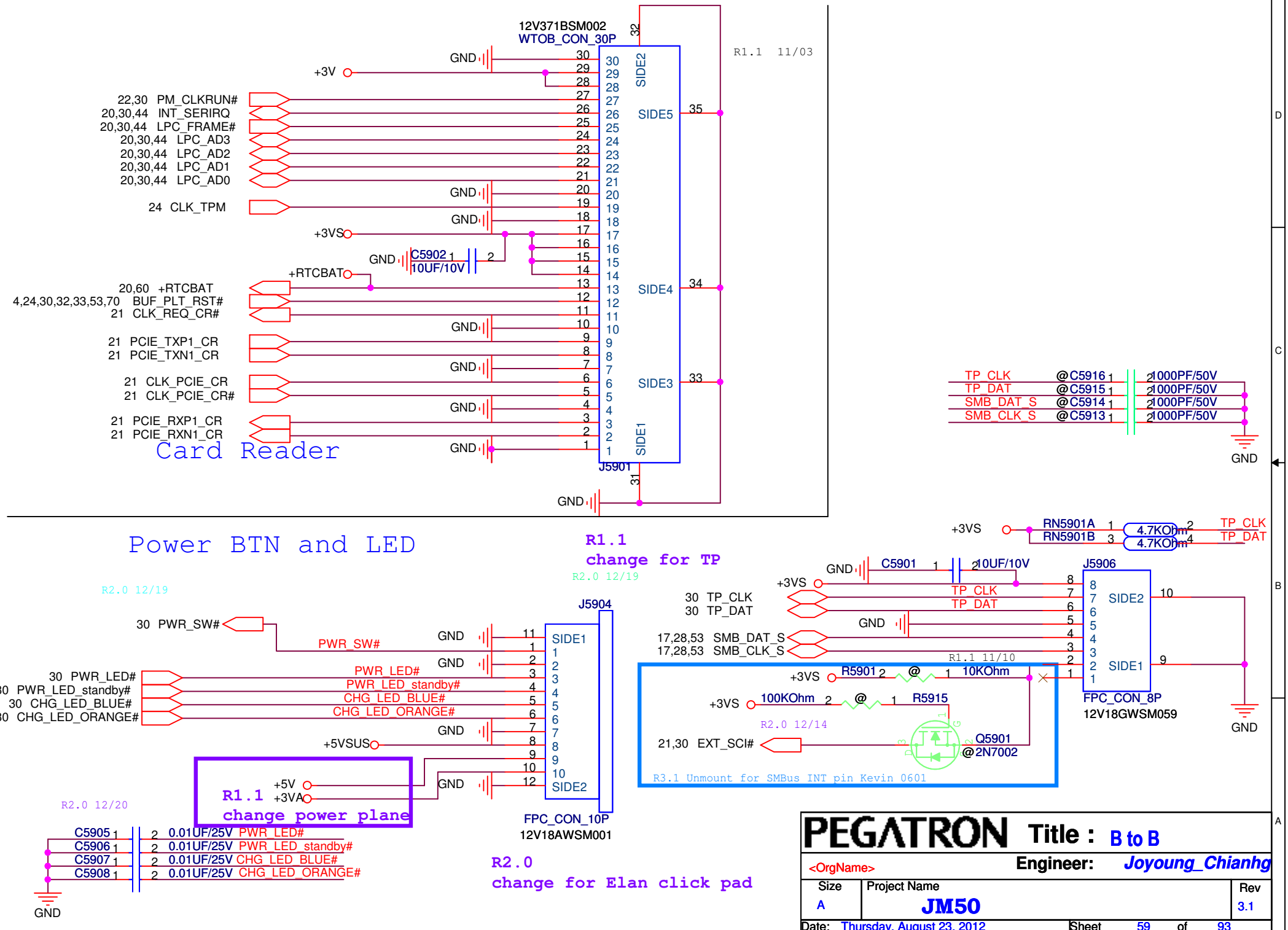
Date: Thursday, August 23, 2012 Sheet 57 of 93

PEGATRON Title : System Setting

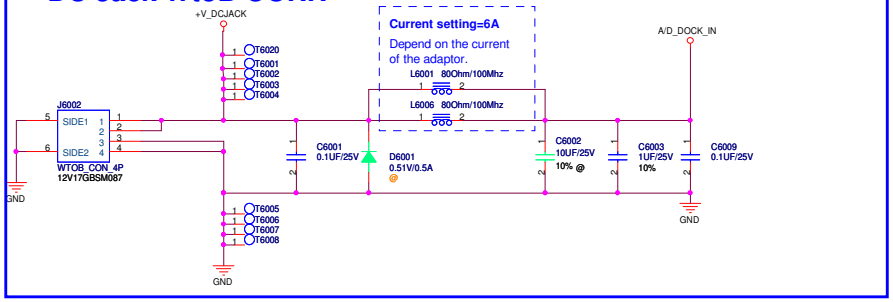
<OrgName> Engineer: Joyoung_Chianhg

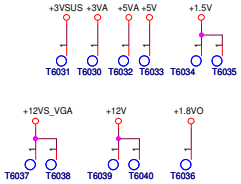
Size	Project Name	Rev
Custom	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 58 of 93


12V371BSM002
WTOB_CON_30P
R1.1 11/03
J5901
SIDE1
SIDE2
SIDE3
SIDE4
SIDE5
22,30 PM_CLKRUN#
20,30,44 INT_SERIRQ
20,30,44 LPC_FRAME#
20,30,44 LPC_AD3
20,30,44 LPC_AD2
20,30,44 LPC_AD1
20,30,44 LPC_AD0
24 CLK_TPM
+3V
+3VS
GND
C5902 10UF/10V
+RTCBAT
20,60 +RTCBAT
4,24,30,32,33,53,70 BUF_PLT_RST#
21 CLK_REQ_CR#
21 PCIE_TXP1_CR
21 PCIE_TXN1_CR
21 CLK_PCIE_CR
21 CLK_PCIE_CR#
21 PCIE_RXP1_CR
21 PCIE_RXN1_CR
Card Reader
TP_CLK @C5916 1000PF/50V
TP_DAT @C5915 1000PF/50V
SMB_DAT_S @C5914 1000PF/50V
SMB_CLK_S @C5913 1000PF/50V
Power BTN and LED
R2.0 12/19
30 PWR_SW#
30 PWR_LED#
30 PWR_LED_standby#
30 CHG_LED_BLUE#
30 CHG_LED_ORANGE#
PWR_SW#
PWR_LED#
PWR_LED_standby#
CHG_LED_BLUE#
CHG_LED_ORANGE#
+5VSUS
+5V
+3VA
R1.1
change power plane
J5904
FPC_CON_10P
12V18AWSM001
R2.0 12/20
C5905 0.01UF/25V PWR_LED#
C5906 0.01UF/25V PWR_LED_standby#
C5907 0.01UF/25V CHG_LED_BLUE#
C5908 0.01UF/25V CHG_LED_ORANGE#
R1.1
change for TP
R2.0 12/19
R2.0
change for Elan click pad
RN5901A 4.7KOhm
RN5901B 4.7KOhm
TP_CLK
TP_DAT
C5901 10UF/10V
30 TP_CLK
30 TP_DAT
17,28,53 SMB_DAT_S
17,28,53 SMB_CLK_S
R1.1 11/10
R5901 10KOhm
R5915 100KOhm
21,30 EXT_SCI#
Q5901 @2N7002
R2.0 12/14
R3.1 Unmount for SMBus INT pin Kevin 0601
J5906
FPC_CON_8P
12V18GWSM059
PEGATRON
Title : B to B
<OrgName>
Engineer: Joyoung_Chianhg
Size A
Project Name JM50
Rev 3.1
Date: Thursday, August 23, 2012
Sheet 59 of 93

DC Jack WtoB CONN





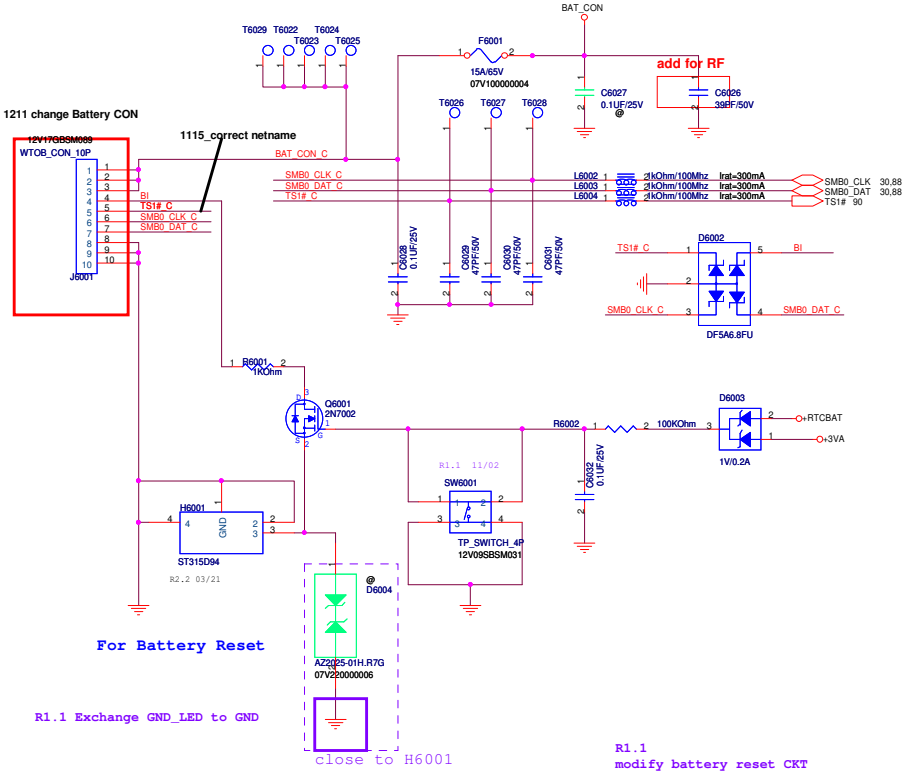
+VCC_RTC +VCC_RTC 20,22,27
+3VA_EC +3VA_EC 28,30,32
+3VA +3VA 6,20,26,27,30,31,57,59,81,88,93
+5VA +5VA 37,81,91
+3VSUS +3VSUS 4,22,24,28,30,81,92
+5VSUS +5VSUS 51,57,59,91
+12VSUS +12VSUS 28,51,81,91
+1.5V +1.5V 5,16,17,18,57,83
+3V +3V 24,45,57,59,61,91
+5V +5V 57,59,91
+12V +12V 91
+0.75VS +0.75VS 16,17,57,83
+1.05VS +1.05VS 26,27,57,82,87
+1.5VS +1.5VS 7,26,53,57,91
+1.8VS +1.8VS 7,25,26,57,80,84
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+5VS +5VS 27,31,36,37,45,48,50,51,57,80,87,91
+12VS +12VS 28,36,48,91

AC_BAT_SYS AC_BAT_SYS 45,53,81,87,88
A/D_DOCK_IN A/D_DOCK_IN 88
BAT_CON BAT_CON 88

+VCCP +VCCP 3,4,6,7,30,32,57,82
+VCORE +VCORE 6,9,11,80
+VGFX_CORE +VGFX_CORE 7,9,80
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 20,26,27

+V_VREF_DDR3 +V_VREF_DDR3 16,17,18

Battery Connector



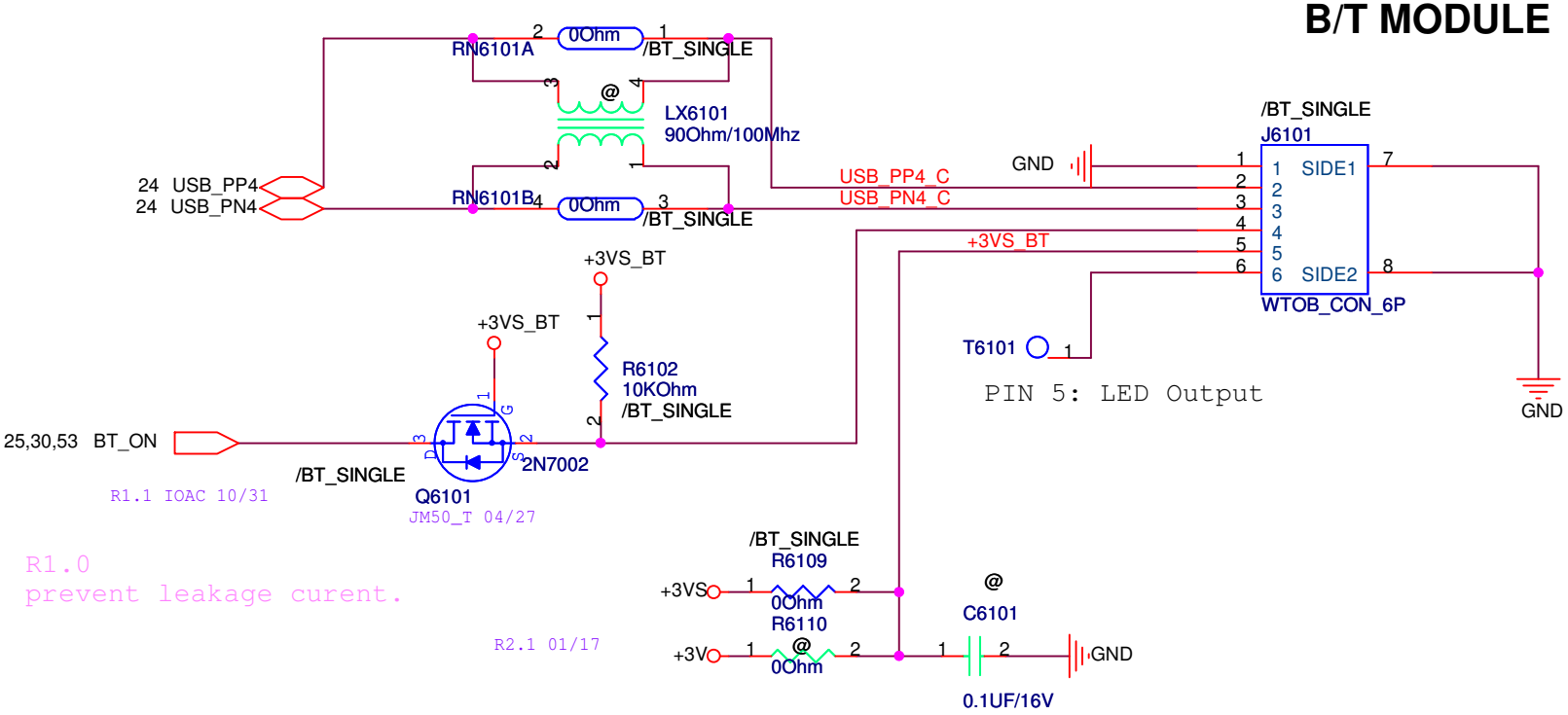
PEGATRON Title : DC_DC/BAT CONN

<OrgName> Engineer: Joyoung_Caianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 60 of 93

B/T MODULE



PEGATRON	Title : Fersco USB 3.0		
Pegatron Corp.	Engineer: Joyoung_Chianhg		
Size: A	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 61 of 93		

PEGATRON Title : System Setting

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 62 of 93

PEGATRON

Title : B to B

<OrgName>

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
A	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 63 of 93

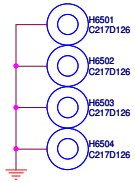
PEGATRON Title : B to B

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

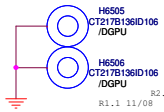
Date: Thursday, August 23, 2012 Sheet 64 of 93

CPU Bracket Hole



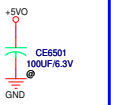
ME B Type

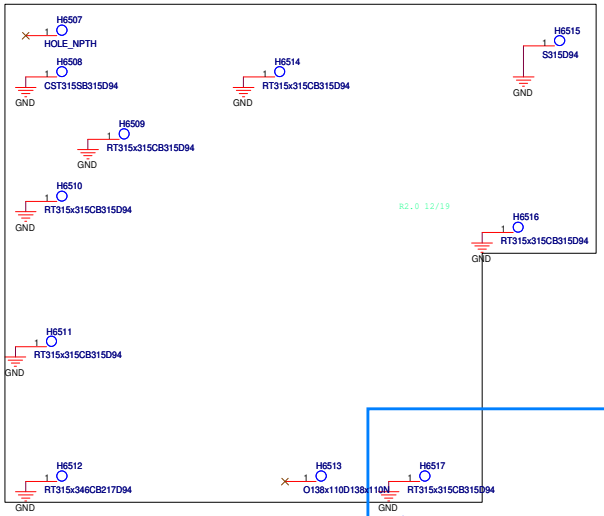
VGA Bracket Hole



R2.0 12/15
R1.1 11/08

place between J5204 /J5205





This screw hole should be Upside down(TOP and BOTTOM).

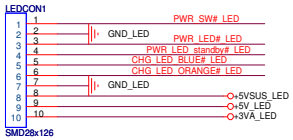
PEGATRON Title : ME_CONN,Skew Hole

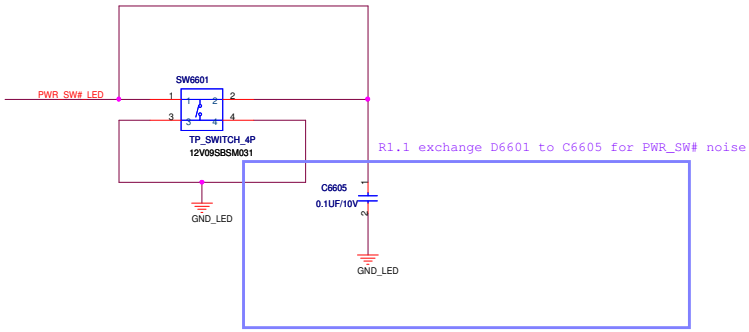
<OrgName> Engineer: Joyoung_Chianhg

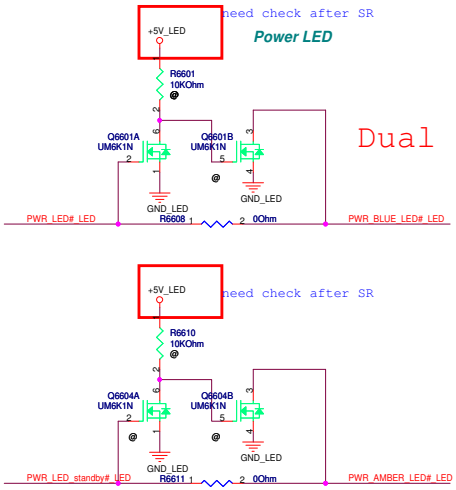
Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 65 of 93

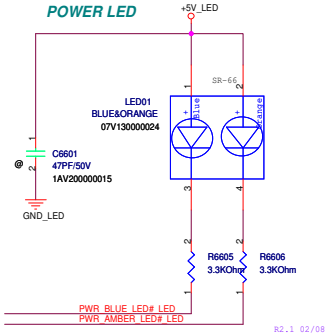
Power Button

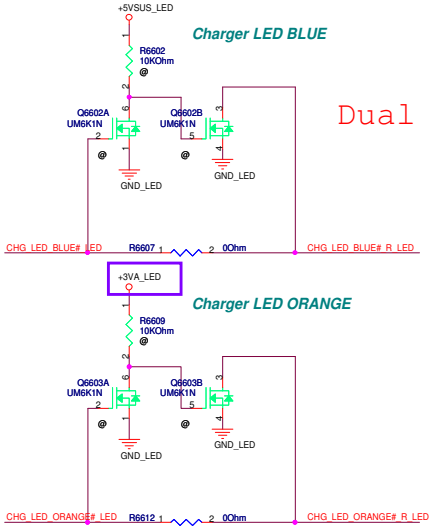




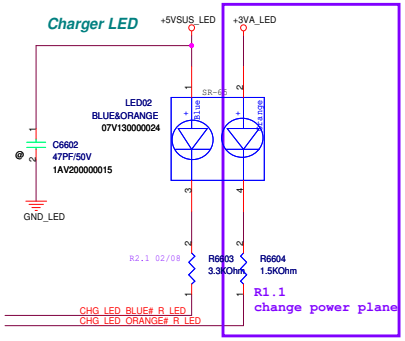


Dual Color

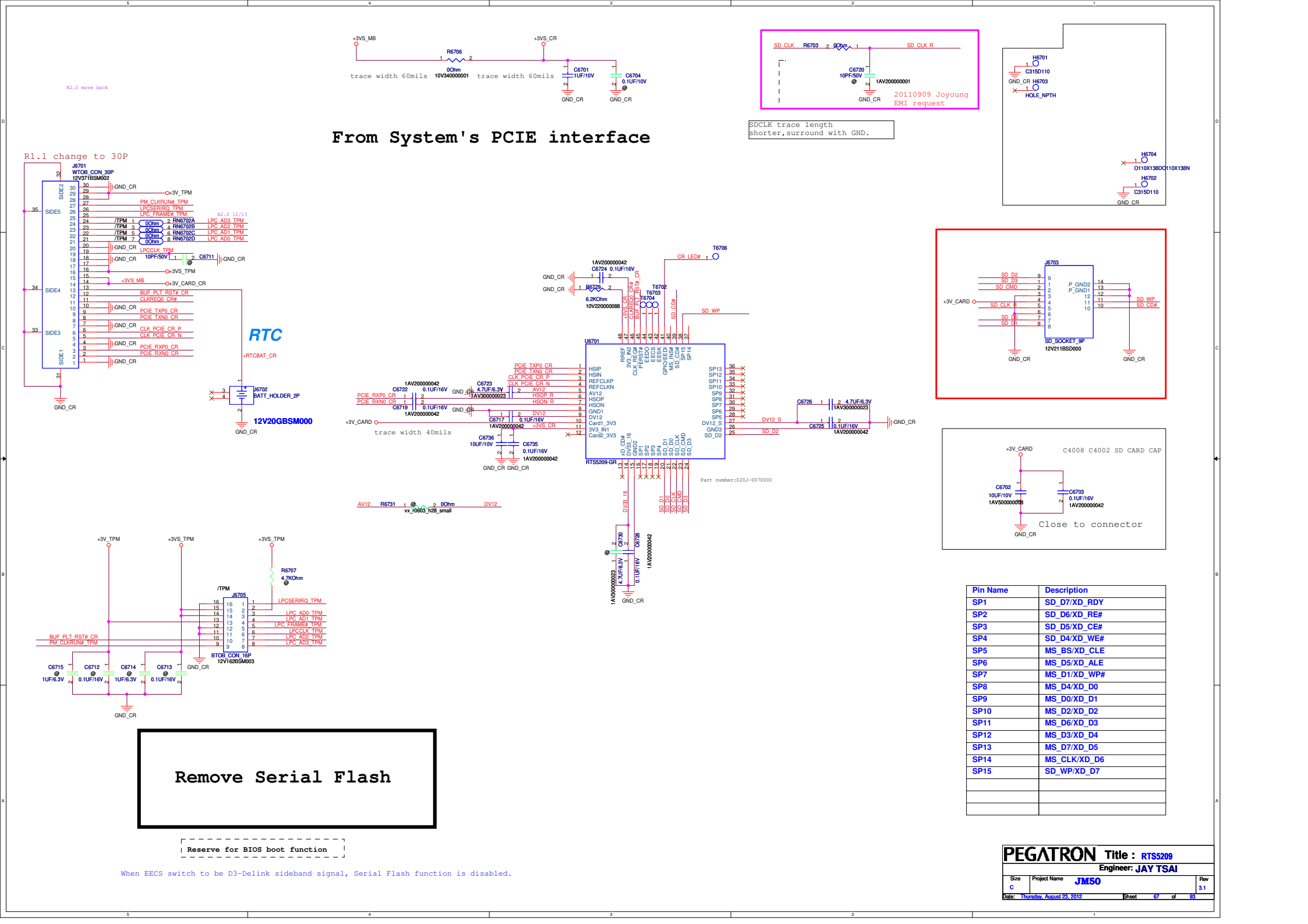




Dual Color



PEGATRON	Title : TP_M		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 66 of 93		



Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

PEGATRON Title : RTS5209
Engineer: JAY TSAI
Size: C | Project Name: JM50 | Rev: 3.1
Date: Thursday, August 23, 2012 | Sheet 67 of 93

PEGATRON

Title : USB_USB Port

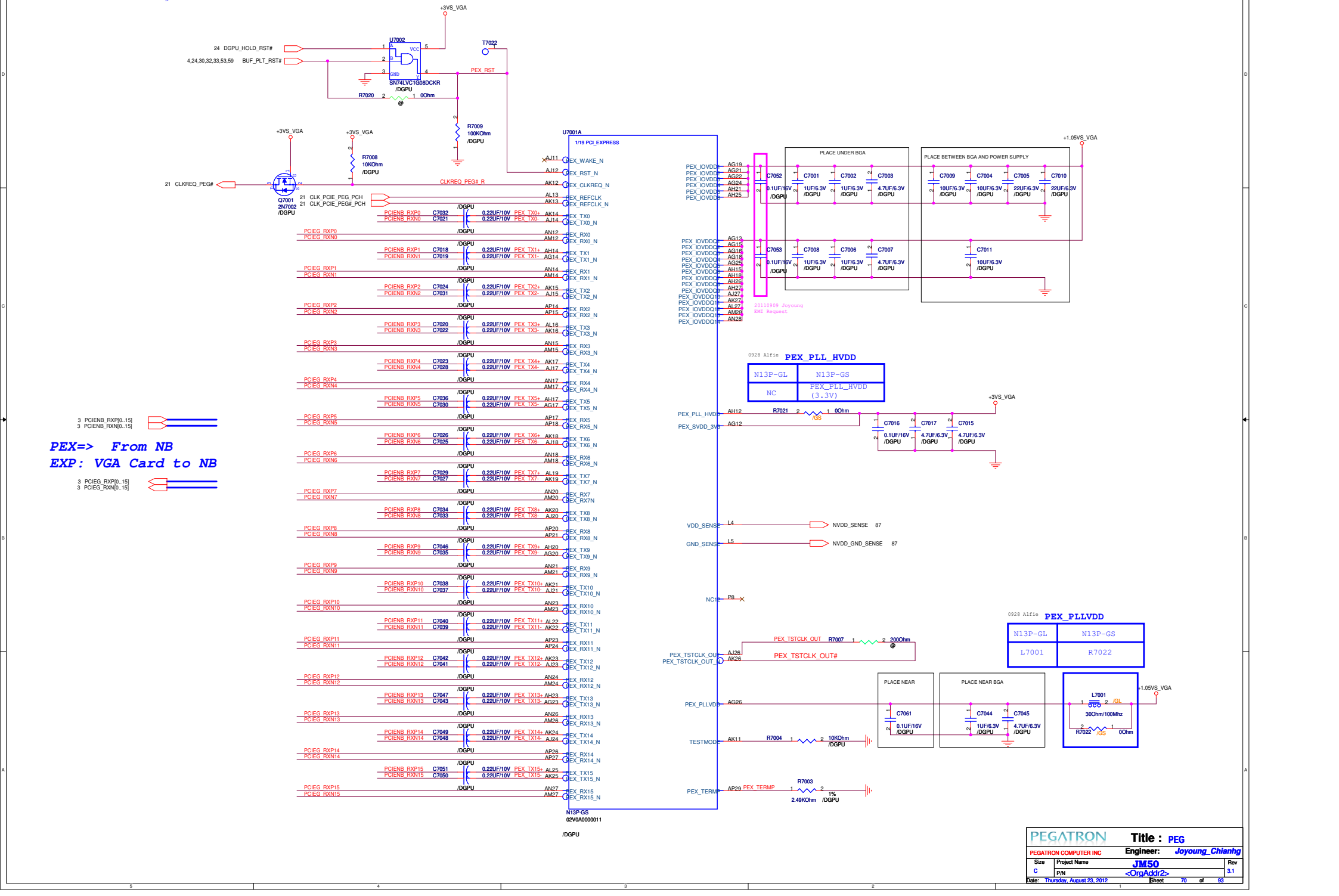
<OrgName>

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 69 of 93

Frank
20110513 Change N13P GPU.

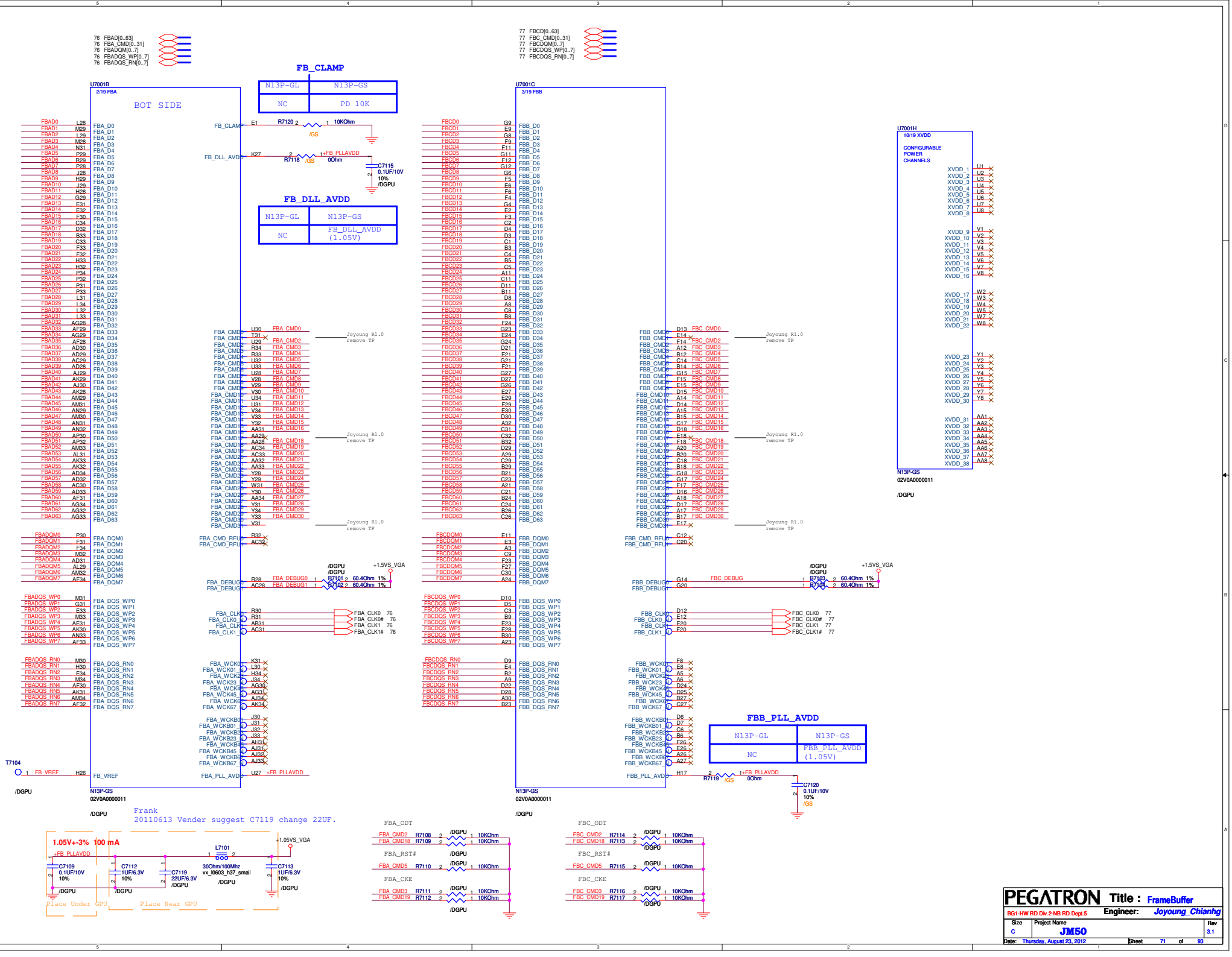


PEGATRON
PEGATRON COMPUTER INC

Title : PEG
Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1
	P/N <OrgAddr2>	

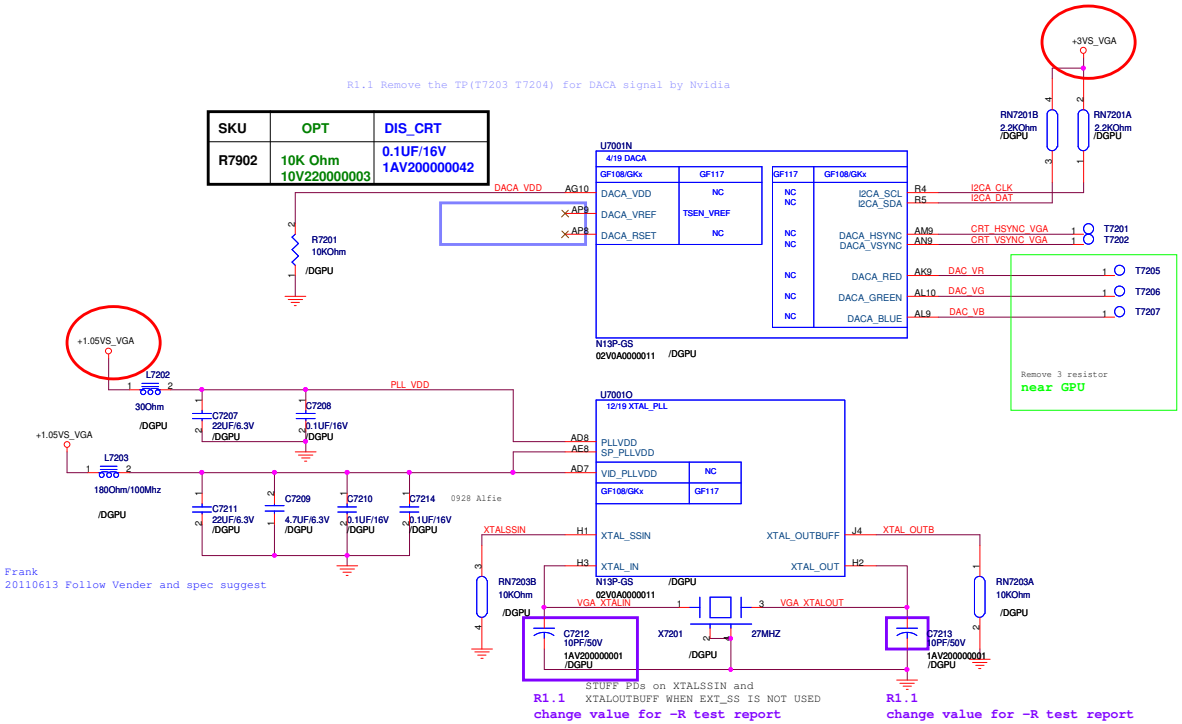
Date: Thursday, August 23, 2012 Sheet 70 of 93



PEGATRON	Title : FrameBuffer
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg
Size: C	Project Name: JM50
Rev: 3.1	
Date: Thursday, August 23, 2012	Sheet 71 of 93

R1.1 Remove the TP(T7203 T7204) for DACA signal by Nvidia

SKU	OPT	DIS_CRT
R7902	10K Ohm 10V220000003	0.1UF/16V 1AV200000042



Frank
20110613 Follow Vender and spec suggest

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

R1.1 change value for -R test report

R1.1 change value for -R test report

PEGATRON	Title : FRAME BUFFER C		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
	P/N: <OrgAddr2>		
Date: Thursday, August 23, 2012	Sheet 72 of 93		

R1.1 Remove the TP (T7301 T7311 T7302 T7307 T7303 T7304 T7305 T7306 T7318 T7309 T7310) by Nvidia

LVDS

U7001J
6/19 IFPAB
ALL PINS NC FOR GF117

IFPAB_RSET AJ8
IFPAB_PLLVDD AH8
IFPA_IOVDD AG8
IFPB_IOVDD AG9

IFPA_TXC AN6 / AM6
IFPA_TXD0 AN3 / AP3
IFPA_TXD1 AM5 / AN5
IFPA_TXD2 AK6 / AL6
IFPA_TXD3 AH6 / AJ6
IFPB_TXC AH9 / AJ9
IFPB_TXD4 AP5 / AP6
IFPB_TXD5 AL7 / AM7
IFPB_TXD6 AM8 / AN8
IFPB_TXD7 AL8 / AK8
GPIO18 N4

IFPAB
N13P-GS
02V0A0000011
/DGPU

Place Under GPU
IFPAB_PLLVDD — R7305 10KOhm /DGPU
IFPAB_IOVDD — R7306 10KOhm /DGPU

HDMI

U7001K
7/19 IFPC
ALL PINS NC FOR GF117

IFPC_RSET AF8
IFPC_PLLVDD AF7
IFPC_IOVDD AF6

DVI/HDMI: I2CW_SDA, I2CW_SCL, TXC, TXC, TXD0, TXD0, TXD1, TXD1, TXD2, TXD2
DP: IFPC_AUX_I2CW_SDA AG2 / IFPC_AUX_I2CW_SCL AG3
IFPC_L3 AG4 / AG5
IFPC_L2 AH4 / AH3
IFPC_L1 AJ2 / AJ3
IFPC_L0 AJ1 / AK1
GPIO15 P2

IFPC
N13P-GS
02V0A0000011
/DGPU

Place Under GPU
IFPC_PLLVDD — R7303 10KOhm /DGPU
IFPC_IOVDD — R7304 10KOhm /DGPU
HDMI_HP Pull-Down 10K at connnector

U7001L
8/19 IFPD
ALL PINS NC FOR GF117

IFPD_RSET AN2
IFPD_PLLVDD AG7
IFPD_IOVDD AG6

DVI/HDMI: I2CX_SDA, I2CX_SCL, TXC, TXC, TXD0, TXD0, TXD1, TXD1, TXD2, TXD2
DP: IFPD_AUX_I2CX_SDA AK2 / IFPD_AUX_I2CX_SCL AK3
IFPD_L3 AK5 / AK4
IFPD_L2 AL4 / AL3
IFPD_L1 AM4 / AM3
IFPD_L0 AM2 / AM1
GPIO17 M6

IFPD
N13P-GS
02V0A0000011
/DGPU

IFPD_PLLVDD — R7308 10KOhm /DGPU
IFPD_IOVDD — R7309 10KOhm /DGPU

U7001M
9/19 IFPEF
ALL PINS NC FOR GF117

IFPEF_PLLVDD AB8
IFPEF_RSET AD6
IFPE_IOVDD AC7
IFPF_IOVDD AC8

DVI-DL / DVI-SL/HDMI / DP

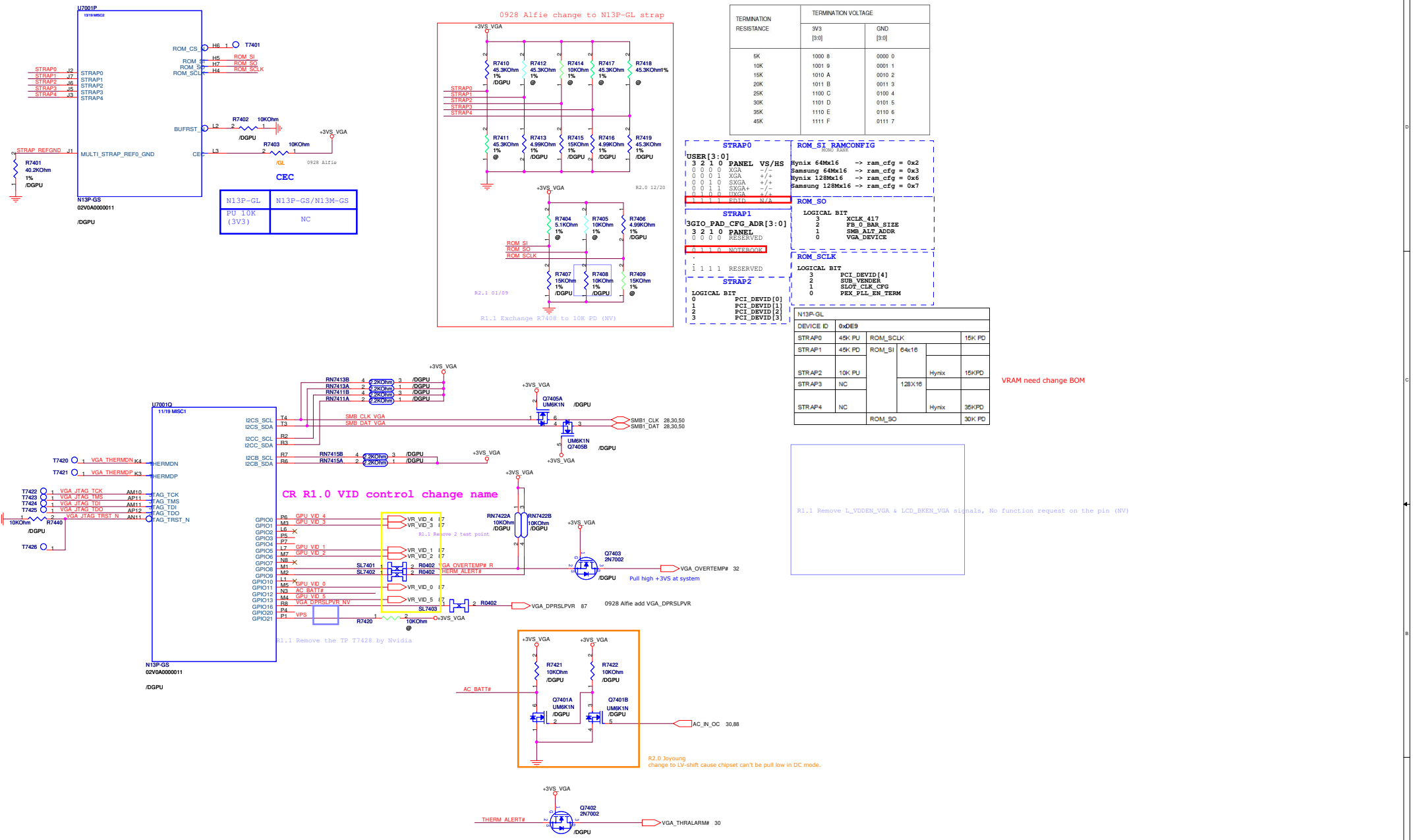
IFPE
I2CY_SDA, I2CY_SCL
TXC, TXC
TXD0, TXD0
TXD1, TXD1
TXD2, TXD2
HPD_E
IFPE_AUX_I2CY_SDA AB4 / IFPE_AUX_I2CY_SCL AB3
IFPE_L3 AC5 / AC4
IFPE_L2 AC3 / AC2
IFPE_L1 AC1 / AD1
IFPE_L0 AD3 / AD2
GPIO16 R1

IFPF
I2CZ_SDA, I2CZ_SCL
TXC, TXC
TXD3, TXD3
TXD4, TXD4
TXD5, TXD5
HPD_F
IFPF_AUX_I2CZ_SDA AF2 / IFPF_AUX_I2CZ_SCL AF3
IFPF_L3 AF1 / AG1
IFPF_L2 AD5 / AD4
IFPF_L1 AF5 / AF4
IFPF_L0 AE4 / AE3
GPIO19 P3

N13P-GS
02V0A0000011
/DGPU

IFPE_PLLVDD — R7312 10KOhm /DGPU
IFPE_IOVDD — R7310 10KOhm /DGPU

PEGATRON	Title : FRAME BUFFER C		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
	P/N: <OrgAddr2>		
Date: Thursday, August 23, 2012	Sheet 73 of 93		



PEGATRON	Title :	FRAME BUFFER A
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg
Size: A2	Project Name: JM50	Rev: 3.1
	P/N: <OrgAddr2>	
Date: Thursday, August 23, 2012	Sheet 74 of 93	

+VGA_VCORE

U7001E
14/19 NVVDD

PLACE UNDER GPU

C7511 C7510 C7513 C7512 C7515 C7514 C7517 C7516 — 0.1UF/16V /DGPU

C7519 C7518 C7521 C7520 C7523 C7522 C7525 C7524 — 4.7UF/6.3V /DGPU

C7527 C7526 C7528 C7529 C7531 C7530 C7532 — 4.7UF/6.3V /DGPU

0928 Alfie change 15pcs 10uF to 4.7uF , follow NV suggest

CE7501 330UF/2V 1BV080000010

C7534 C7533 C7535 C7536 C7537 — 4.7UF/6.3V /DGPU

C7552 — 22UF/6.3V /DGPU

C7553 — 47UF/4V /DGPU

PLACE NEAR GPU

0929 Alfie change 5pcs 10uF to 4.7uF , follow NV suggest

N13P-GS
02V0A0000011
/DGPU

U7001F
18/19 NC/VDD33

Frank
20110613 Follow Vender and spec suggest=>Remove C7506, C7508

C7507 C7501 C7504 C7505 — 0.1UF/16V /DGPU — PLACE NEAR BALLS

C7502 — 1UF/6.3V /DGPU

C7503 — 4.7UF/6.3V /DGPU — PLACE NEAR BGA

+3VS_VGA
R7501 0Ohm /DGPU

N13P-GS
02V0A0000011
/DGPU

Frank
20110613 Follow Vender and spec suggest
=> Add C7542, C7543, C7544, C7545 and C7556 mount
Remove C7540, C7561, C7558, C7649
Change C7541, C7557 to 10uF

U7001D
15/19 FBVDDQ

+1.5VS_VGA

C7539 C7559 C7542 C7544 C7538 C7555 C7554 C7541
0.1UF/16V /DGPU — 1UF/6.3V /DGPU — 4.7UF/6.3V /DGPU — 10UF/6.3V /DGPU

C7551 C7556 C7543 C7545 C7560 C7562 C7550 C7557
0.1UF/16V /DGPU — 1UF/6.3V /DGPU — 4.7UF/6.3V /DGPU — 10UF/6.3V /DGPU

CALIBRATION PIN	GDDR5
FB_CALx_PD_VDDQ	40
FB_CALx_PU_GND	40
FB_CALx_TERM_GND	60

FB_VDDQ_SENSE F1 — FBVDDQ_SENSE — T7508
FB_GND_SENSE F2 — FBVDDQ_GND_SENSE — T7509
FB_CAL_PD_VDDQ J27 — FB_CAL_PD_VDDQ
FB_CAL_PU_GND H27 — FB_CAL_PU_GND
FB_CAL_TERM_GND H25 — FB_CAL_TERM_GND

PLACE CLOSE TO GPU BALLS
+1.5VS_VGA
/DGPU R7507 40.2Ohm
/DGPU R7509 42.2Ohm
/DGPU R7510 51.1Ohm 10V220000319

N13P-GS
02V0A0000011
/DGPU

Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm
Joyoung
20110913 Follow Vendor spec PUN-05893-001_v02=>Change R7510 to 51.1 ohm

U7001G
18/19 GND_1/2

U7001I
17/19 GND_2/2

Optional CMD GNDs (2)
NC for 4-Lyr cards

0612 R3.1 EMI

N13P-GS
02V0A0000011
/DGPU

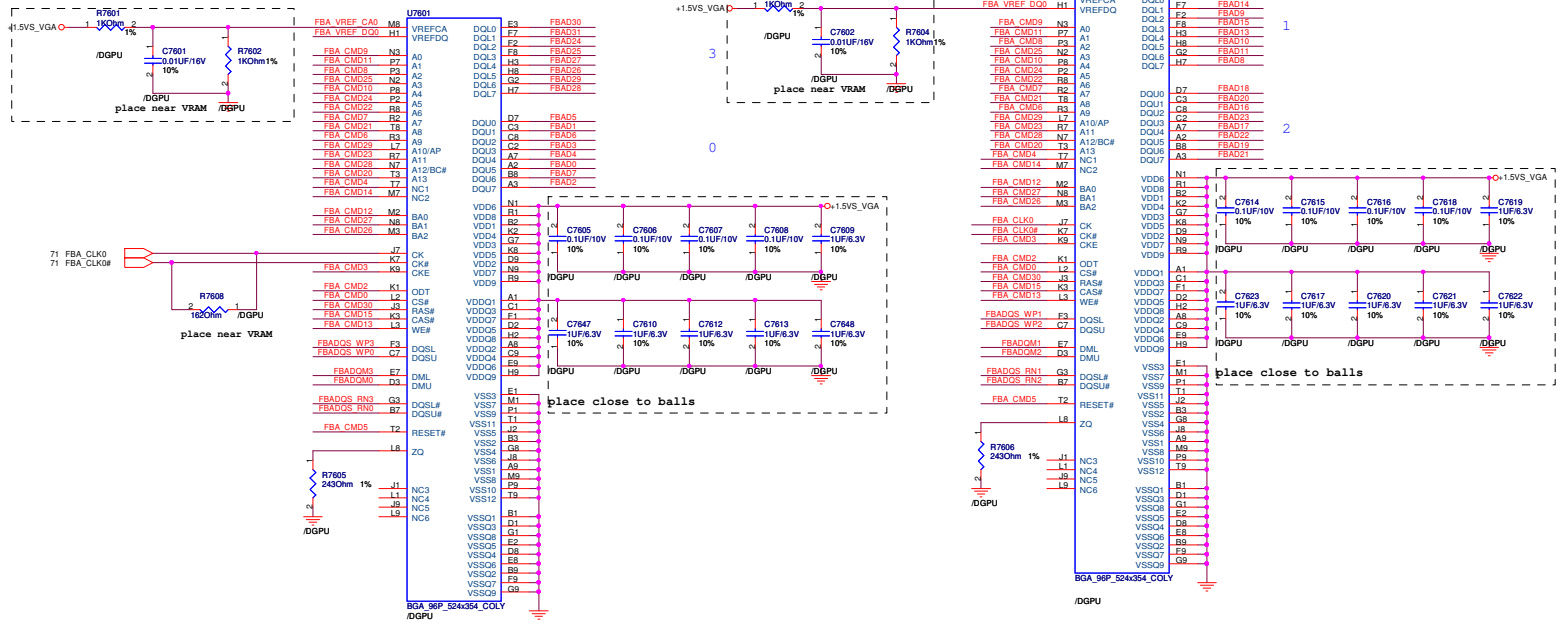
PEGATRON Title : FRAME BUFFER C
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 75 of 93

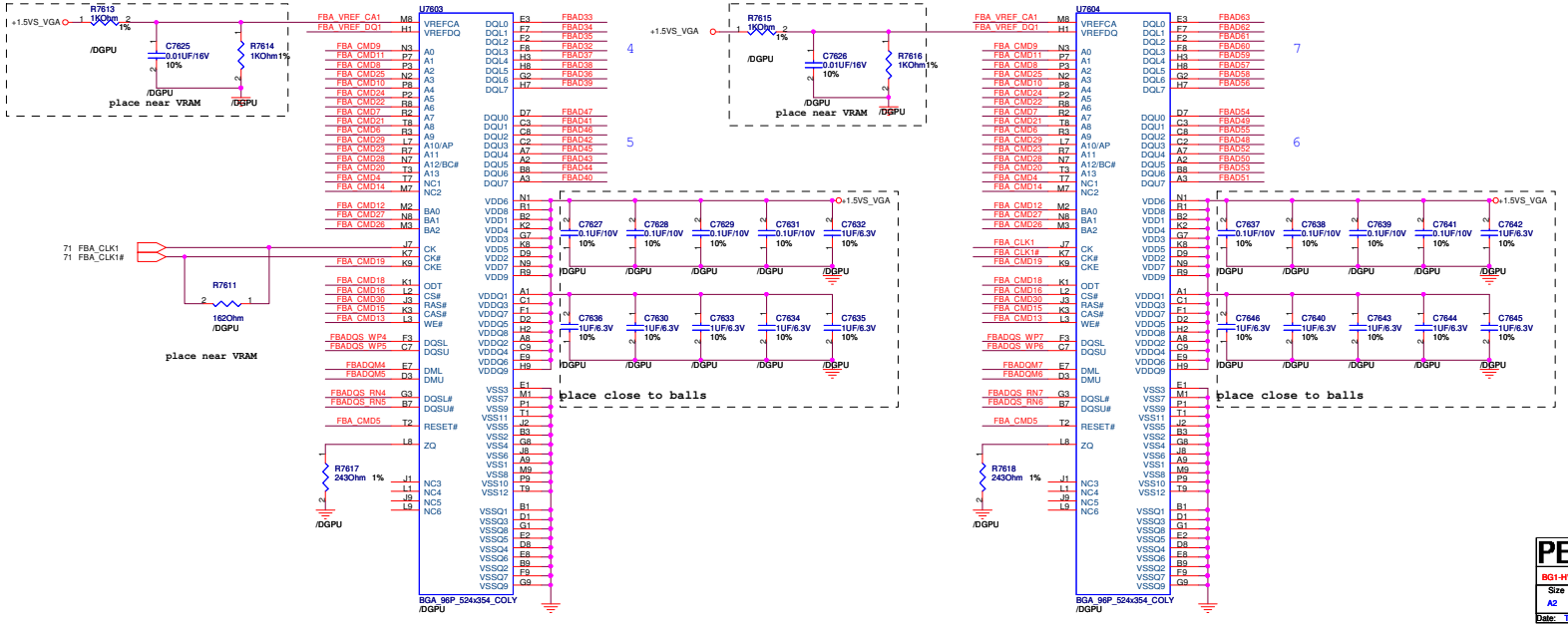
VRAM CH A

TOP SIDE



BOT SIDE

TOP SIDE

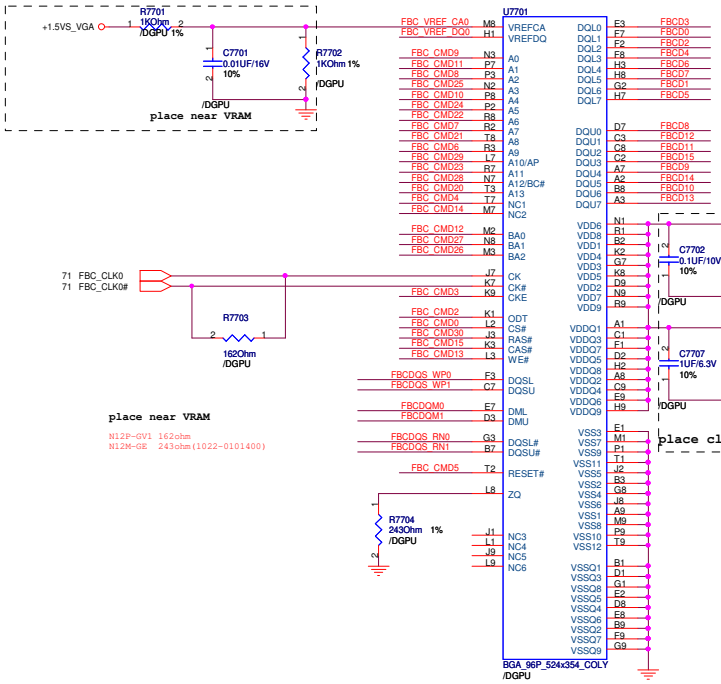


BOT SIDE

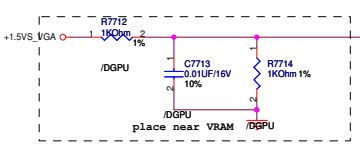
PEGATRON	Title : FRAME BUFFER A	
BG1-HW RD Div.2-NB RD Dep.L5	Engineer: Joyoung_Chianhg	
Size: A2	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 76 of 93	

VRAM CH C

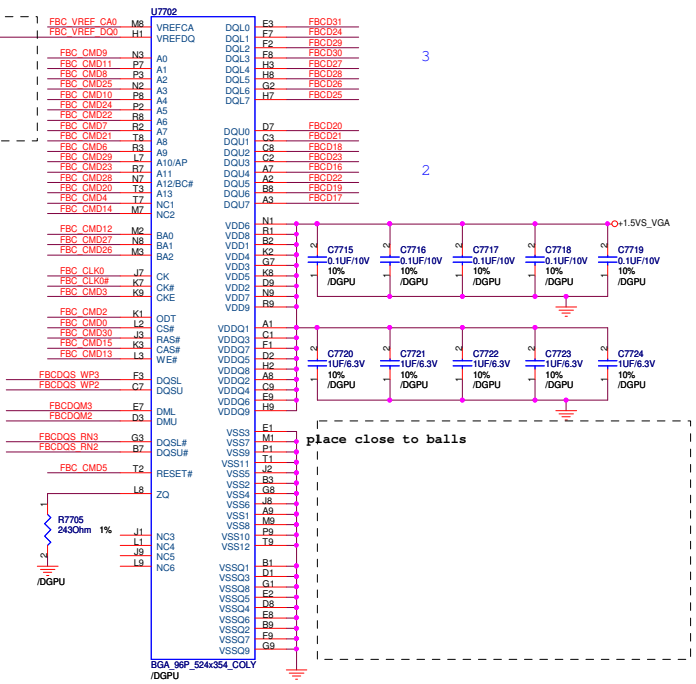
TOP SIDE



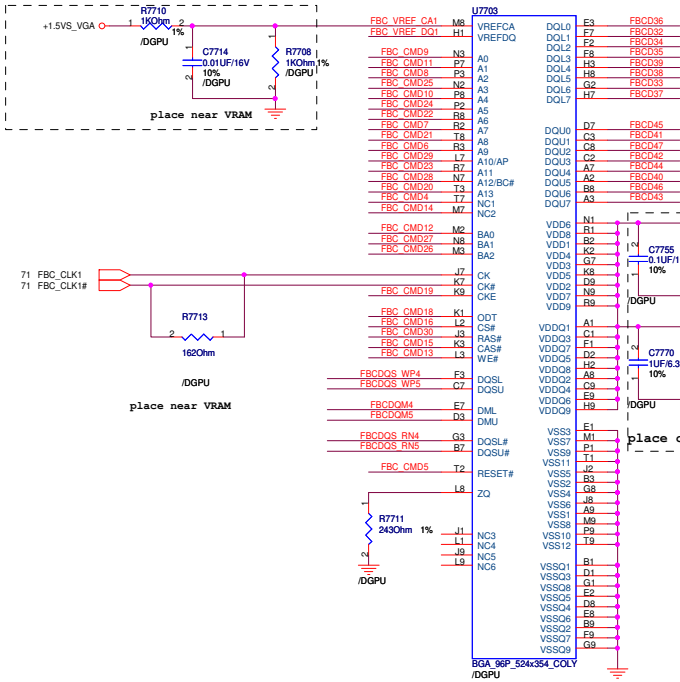
71 FBCD[0..63]
71 FBC_CMD[0..31]
71 FBCDQM[0..7]
71 FBCDQS_WP[0..7]
71 FBCDQS_RN[0..7]

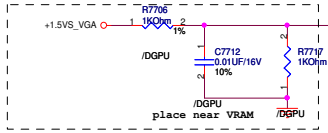


BOT SIDE

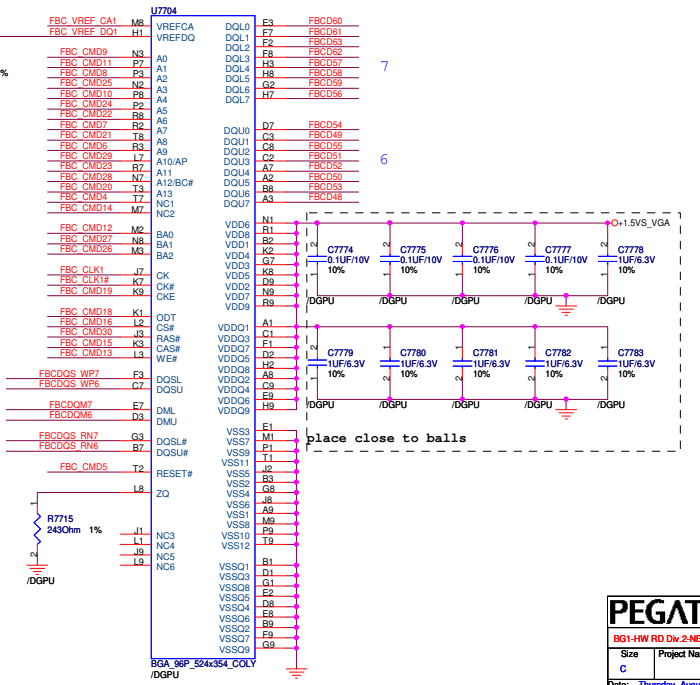


TOP SIDE





BOT SIDE



PEGATRON	Title : FRAME BUFFER B	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 77 of 93	

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1
	P/N <OrgAddr2>	

Date: Thursday, August 23, 2012 Sheet 78 of 93

PEGATRON

Title : GPU PWR/GND

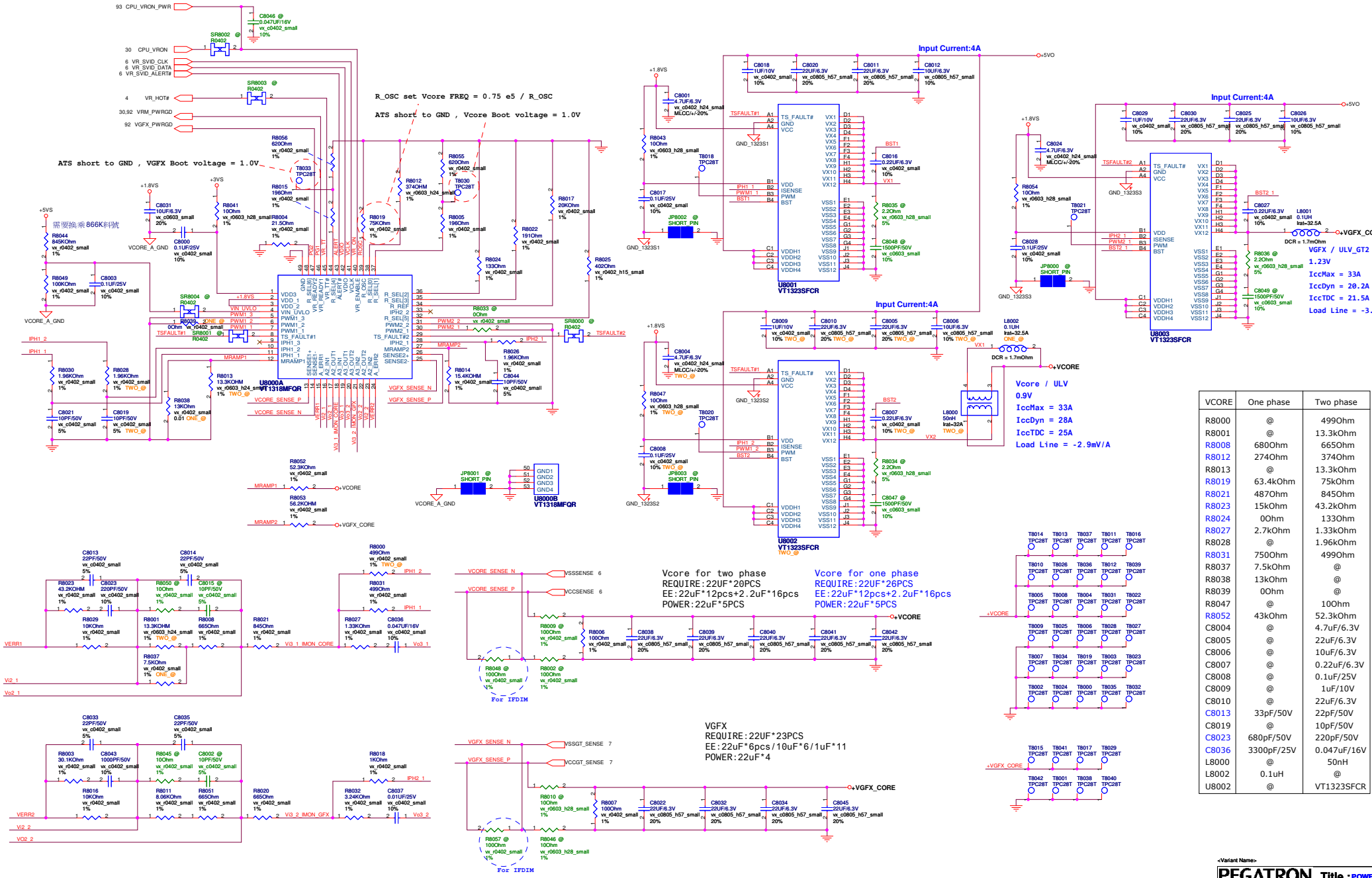
PEGATRON COMPUTER INC

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1
	P/N <OrgAddr2>	

Date: Thursday, August 23, 2012 Sheet 79 of 93

+VCORE & +VGFX POWER SUPPLY



VCORE	One phase	Two phase
R8000	@	499Ohm
R8001	@	13.3kOhm
R8008	680Ohm	665Ohm
R8012	274Ohm	374Ohm
R8013	@	13.3kOhm
R8019	63.4kOhm	75kOhm
R8021	487Ohm	845Ohm
R8023	15kOhm	43.2kOhm
R8024	0Ohm	133Ohm
R8027	2.7kOhm	1.33kOhm
R8028	@	1.96kOhm
R8031	750Ohm	499Ohm
R8037	7.5kOhm	@
R8038	13kOhm	@
R8039	0Ohm	@
R8047	@	10Ohm
R8052	43kOhm	52.3kOhm
C8004	@	4.7uF/6.3V
C8005	@	22uF/6.3V
C8006	@	10uF/6.3V
C8007	@	0.22uF/6.3V
C8008	@	0.1uF/25V
C8009	@	1uF/10V
C8010	@	22uF/6.3V
C8013	33pF/50V	22pF/50V
C8019	@	10pF/50V
C8023	680pF/50V	220pF/50V
C8036	3300pF/25V	0.047uF/16V
L8000	@	50nH
L8002	0.1uH	@
U8002	@	VT1323SFCR

<Variant Name>

PEGATRON Title : POWER_VCORE&VGFX

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

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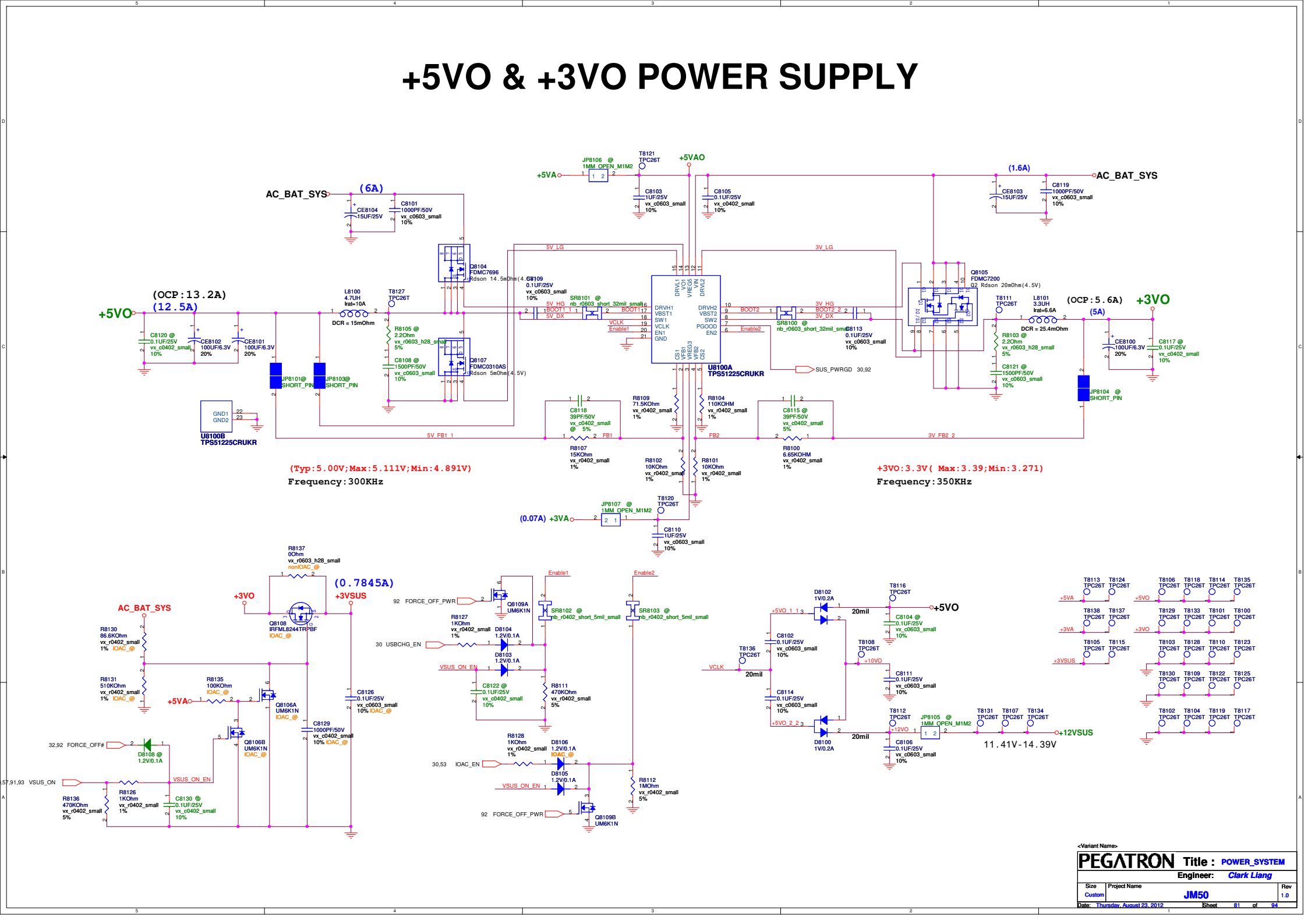
+5VO & +3VO POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_SYSTEM

Engineer: Clark Liang

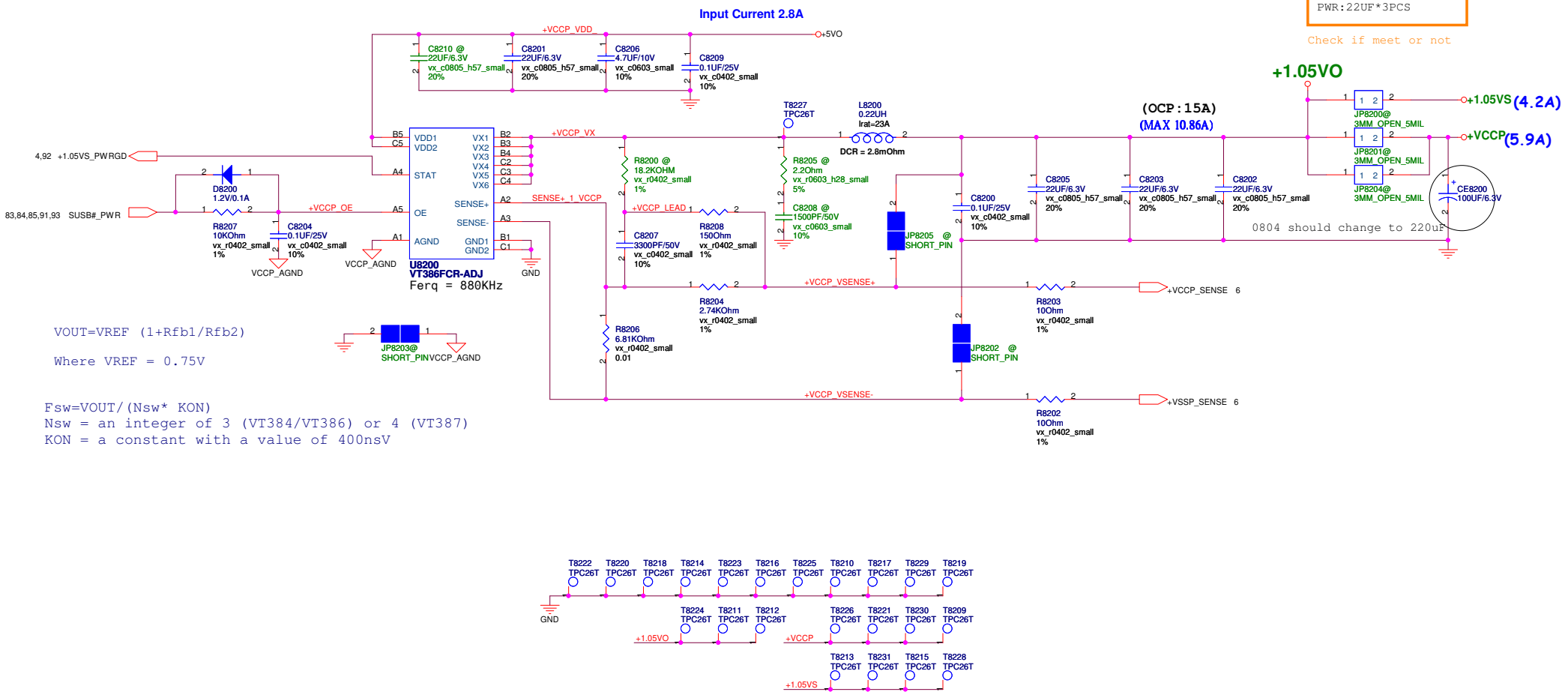
Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 81 of 94

+1.05VO POWER SUPPLY

11/07/21
+1.05VS & +VCCP
REQUIRE:22UF*18PCS
EE:10UF*10PCS/1uF*26
PWR:22UF*3PCS

Check if meet or not



<Variant Name>

PEGATRON Title : POWER_+VCCP

Engineer: Clark Liang

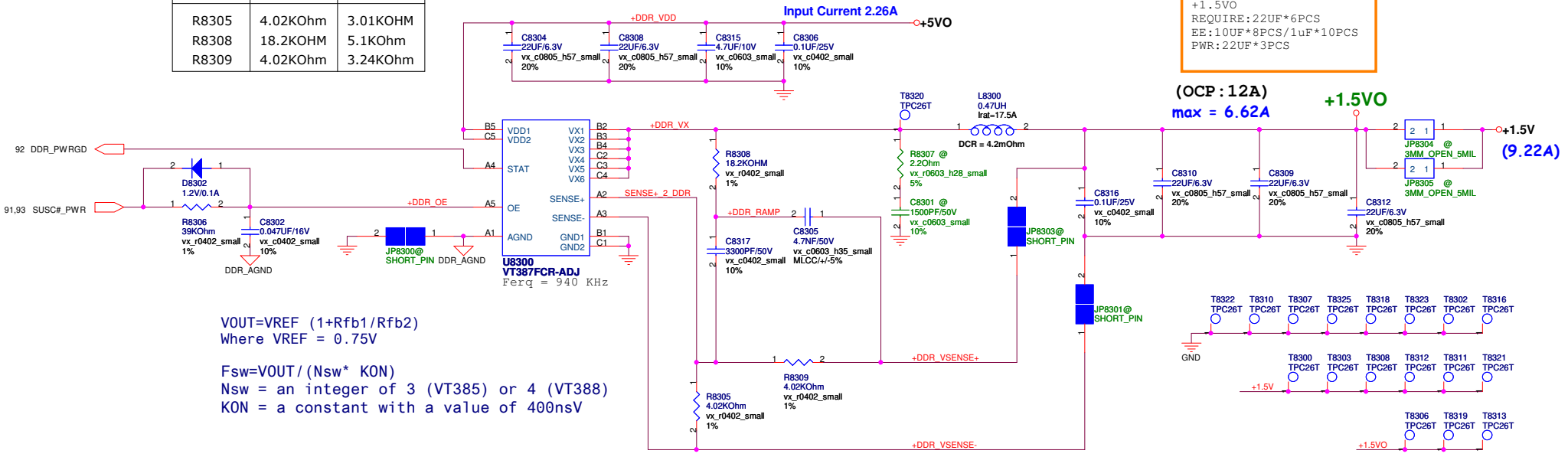
Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 82 of 94

+1.5VO POWER SUPPLY

1.5VO	UMA	DSC
Vout	1.5V	1.557V
R8305	4.02KOhm	3.01KOHM
R8308	18.2KOHM	5.1KOhm
R8309	4.02KOhm	3.24KOhm

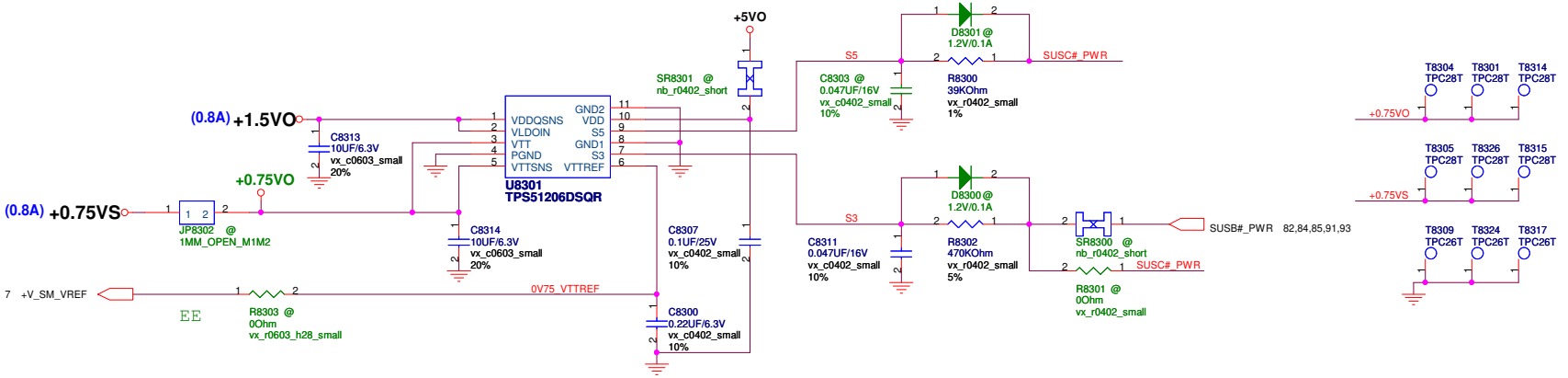
11/07/21
+1.5VO
REQUIRE:22UF*6PCS
EE:10UF*8PCS/1uF*10PCS
PWR:22UF*3PCS



VOUT=VREF (1+Rfb1/Rfb2)
Where VREF = 0.75V

Fsw=VOUT/(Nsw* KON)
Nsw = an integer of 3 (VT385) or 4 (VT388)
KON = a constant with a value of 400nsV

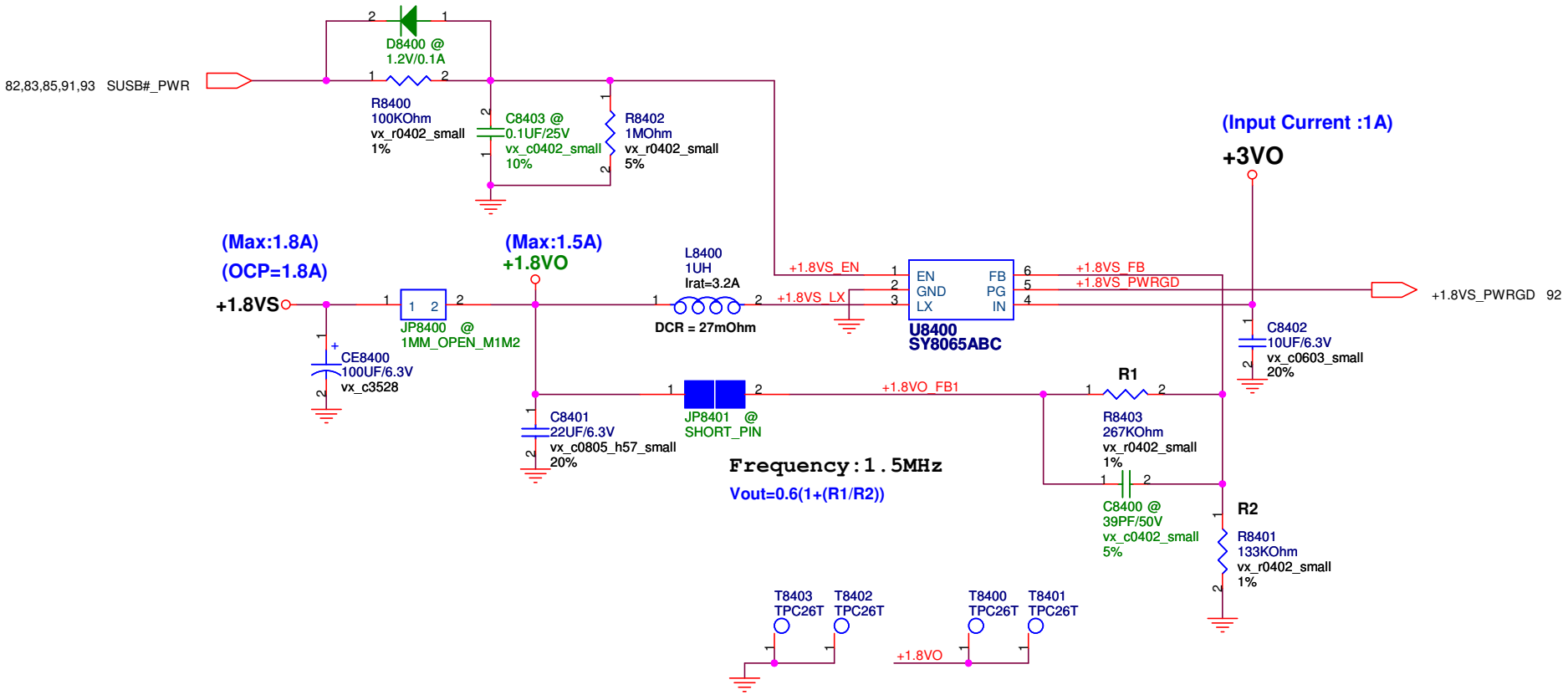
+0.75VS POWER SUPPLY



<Variant Name>

PEGATRON	Title : POWER_DDR & VTT	
	Engineer: Clark Liang	
Size: Custom	Project Name: JM50	Rev: 1.0
Date: Thursday, August 23, 2012	Sheet 83 of 94	

+1.8VS POWER SUPPLY



<Variant Name>

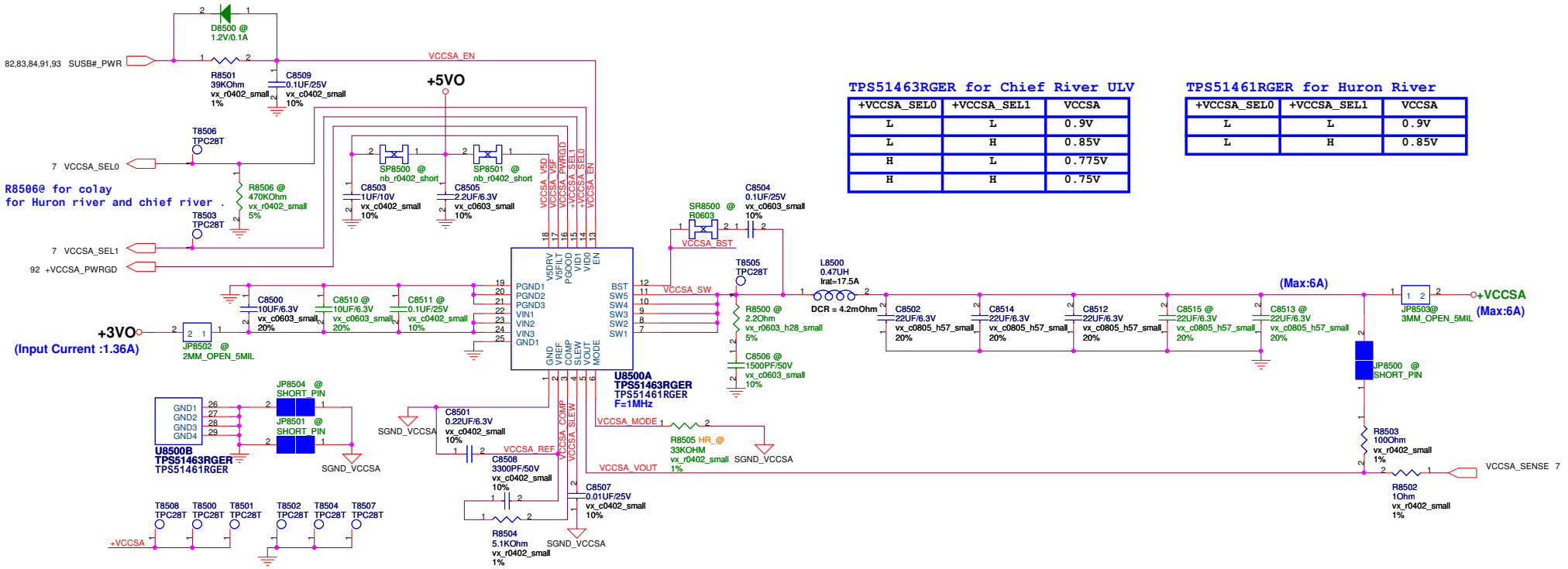
PEGATRON Title : POWER_+1.8VS

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 84 of 94

VCCSA POWER SUPPLY



TPS51463RGER for Chief River ULV

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

TPS51461RGER for Huron River

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V

<Variant Name>

PEGATRON Title :POWER_+VCCSA_0.85VS

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 85 of 94

<Variant Name>

PEGATRON

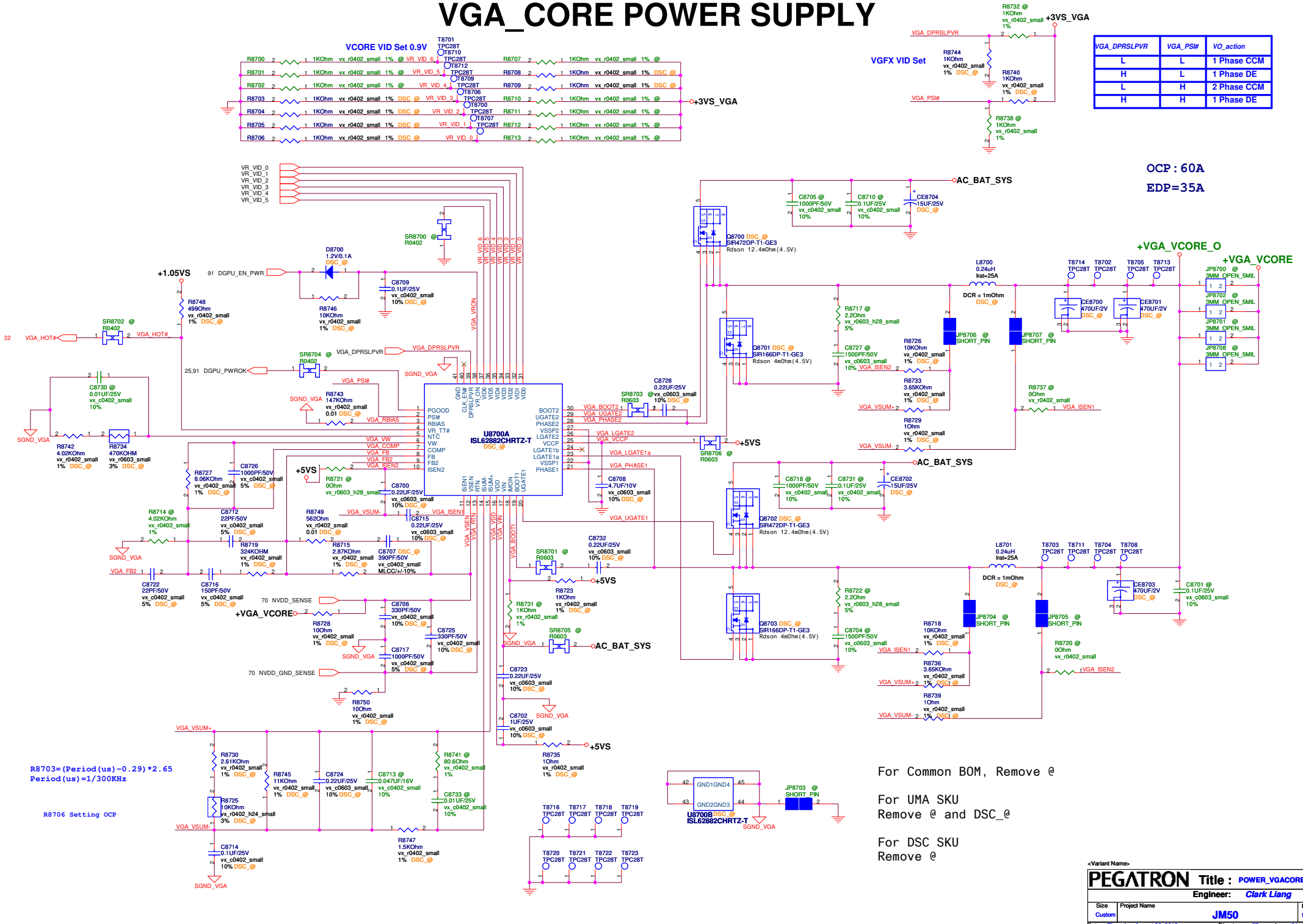
Title : POWER_N/A

Engineer: *Clark Liang*

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 86 of 94

VGA_CORE POWER SUPPLY



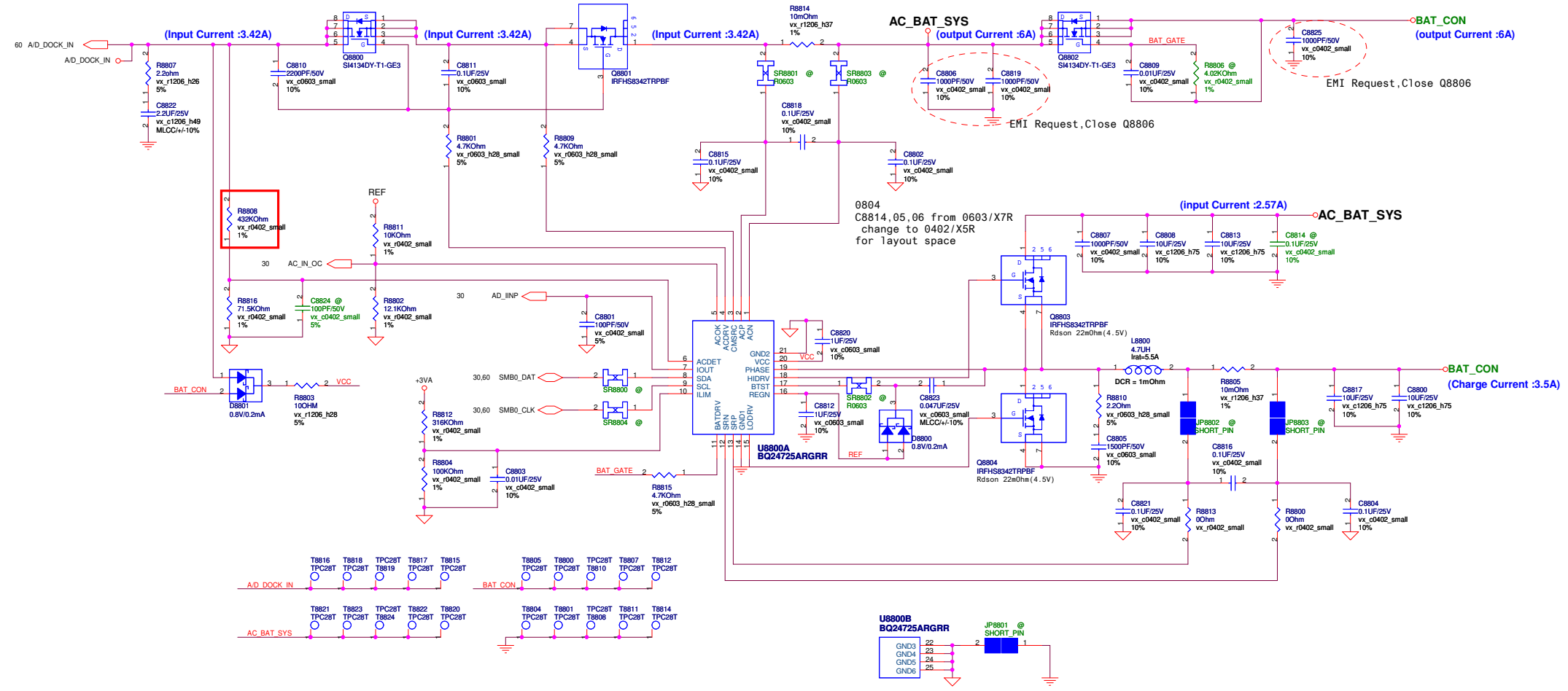
VGA_DPRSLPVR	VGA_PSI#	VO_action
L	L	1 Phase CCM
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

PEGATRON Title : POWER_VGACORE
Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 87 of 94

BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 88 of 94

<Variant Name>

PEGATRON

Title : POWER_N/A

Engineer: *Clark Liang*

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 89 of 94

BATTERY IN DETECT

<Variant Name>

PEGATRON

Title : POWER_DETECT

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

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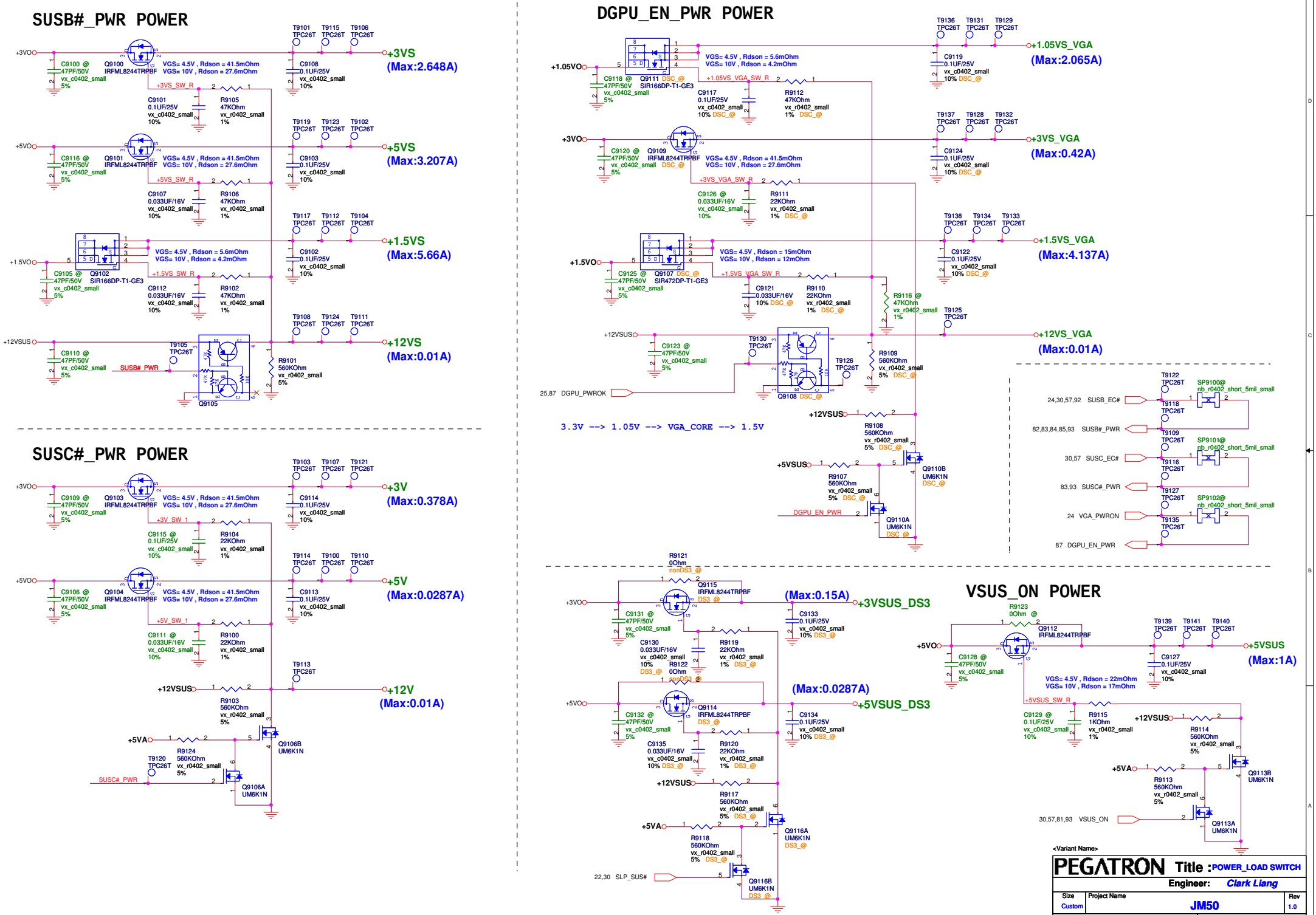
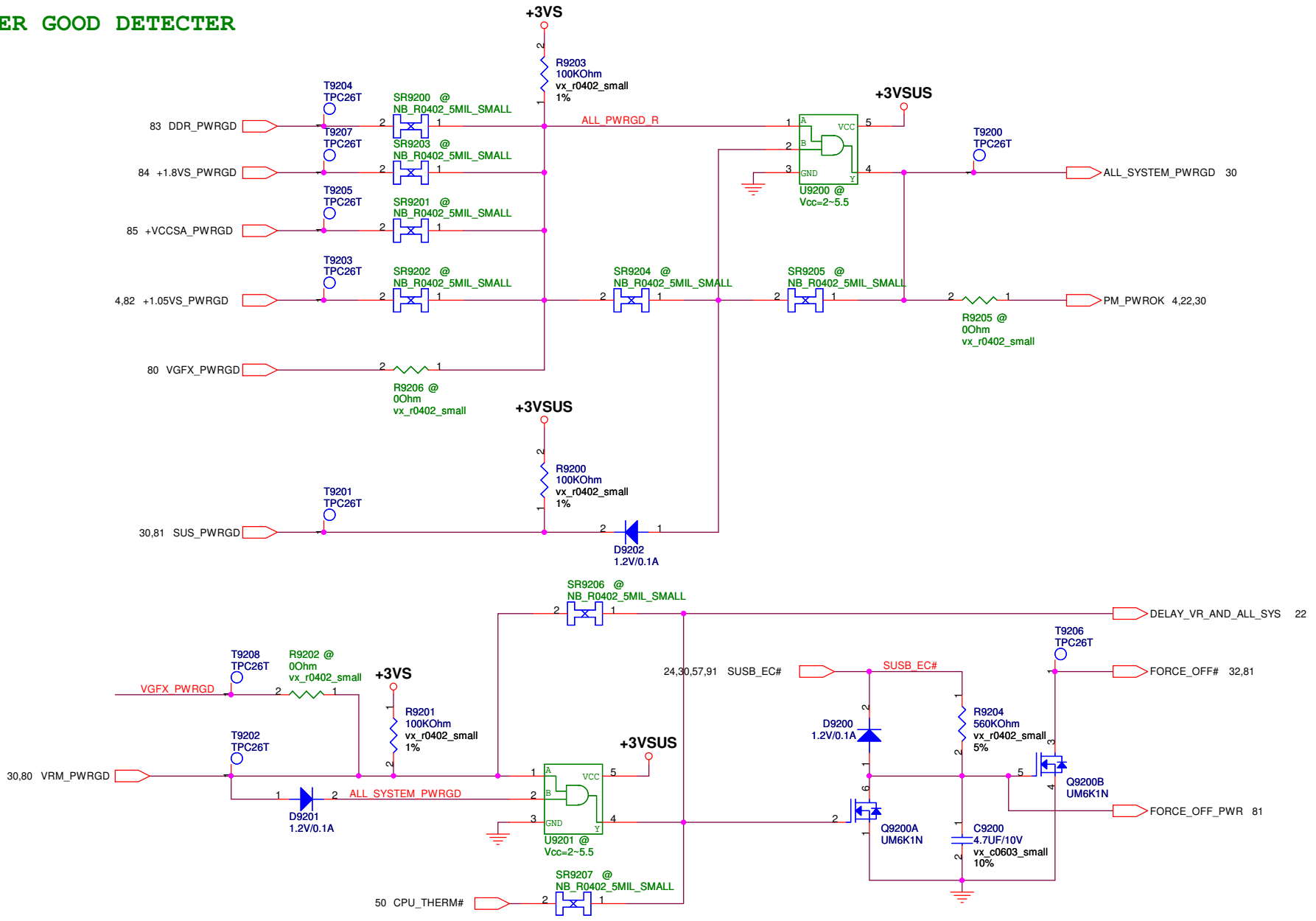

SUSB#_PWR POWER
+3VO
C9100 @ 47PF/50V vx_c0402_small 5%
Q9100 IRFML8244TRPBF
VGS= 4.5V , Rdson = 41.5mOhm
VGS= 10V , Rdson = 27.6mOhm
+3VS_SW_R
C9101 0.1UF/25V vx_c0402_small 10%
R9105 47KOhm vx_r0402_small 1%
T9101 TPC26T T9115 TPC26T T9106 TPC26T
C9108 0.1UF/25V vx_c0402_small 10%
+3VS (Max:2.648A)
+5VO
C9116 @ 47PF/50V vx_c0402_small 5%
Q9101 IRFML8244TRPBF
VGS= 4.5V , Rdson = 41.5mOhm
VGS= 10V , Rdson = 27.6mOhm
+5VS_SW_R
C9107 0.033UF/16V vx_c0402_small 10%
R9106 47KOhm vx_r0402_small 1%
T9119 TPC26T T9123 TPC26T T9102 TPC26T
C9103 0.1UF/25V vx_c0402_small 10%
+5VS (Max:3.207A)
+1.5VO
C9105 @ 47PF/50V vx_c0402_small 5%
Q9102 SIR166DP-T1-GE3
VGS= 4.5V , Rdson = 5.6mOhm
VGS= 10V , Rdson = 4.2mOhm
+1.5VS_SW_R
C9112 0.033UF/16V vx_c0402_small 10%
R9102 47KOhm vx_r0402_small 1%
T9117 TPC26T T9112 TPC26T T9104 TPC26T
C9102 0.1UF/25V vx_c0402_small 10%
+1.5VS (Max:5.66A)
+12VSUS
C9110 @ 47PF/50V vx_c0402_small 5%
SUSB#_PWR
T9105 TPC26T
Q9105
R9101 560KOhm vx_r0402_small 5%
T9108 TPC26T T9124 TPC26T T9111 TPC26T
+12VS (Max:0.01A)
SUSC#_PWR POWER
+3VO
C9109 @ 47PF/50V vx_c0402_small 5%
Q9103 IRFML8244TRPBF
VGS= 4.5V , Rdson = 41.5mOhm
VGS= 10V , Rdson = 27.6mOhm
+3V_SW_1
C9115 @ 0.1UF/25V vx_c0402_small 10%
R9104 22KOhm vx_r0402_small 1%
T9103 TPC26T T9107 TPC26T T9121 TPC26T
C9114 0.1UF/25V vx_c0402_small 10%
+3V (Max:0.378A)
+5VO
C9106 @ 47PF/50V vx_c0402_small 5%
Q9104 IRFML8244TRPBF
VGS= 4.5V , Rdson = 41.5mOhm
VGS= 10V , Rdson = 27.6mOhm
+5V_SW_1
C9111 @ 0.033UF/16V vx_c0402_small 10%
R9100 22KOhm vx_r0402_small 1%
T9114 TPC26T T9100 TPC26T T9110 TPC26T
C9113 0.1UF/25V vx_c0402_small 10%
+5V (Max:0.0287A)
+12VSUS
R9103 560KOhm vx_r0402_small 5%
T9113 TPC26T
+12V (Max:0.01A)
+5VA
R9124 560KOhm vx_r0402_small 5%
T9120 TPC26T
SUSC#_PWR
Q9106A UM6K1N
Q9106B UM6K1N
DGPU_EN_PWR POWER
+1.05VO
C9118 @ 47PF/50V vx_c0402_small 5%
Q9111 DSC_@ SIR166DP-T1-GE3
VGS= 4.5V , Rdson = 5.6mOhm
VGS= 10V , Rdson = 4.2mOhm
+1.05VS_VGA_SW_R
C9117 0.1UF/25V vx_c0402_small 10% DSC_@
R9112 47KOhm vx_r0402_small 1% DSC_@
T9136 TPC26T T9131 TPC26T T9129 TPC26T
C9119 0.1UF/25V vx_c0402_small 10% DSC_@
+1.05VS_VGA (Max:2.065A)
+3VO
C9120 @ 47PF/50V vx_c0402_small 5%
Q9109 IRFML8244TRPBF DSC_@
VGS= 4.5V , Rdson = 41.5mOhm
VGS= 10V , Rdson = 27.6mOhm
+3VS_VGA_SW_R
C9126 @ 0.033UF/16V vx_c0402_small 10%
R9111 22KOhm vx_r0402_small 1% DSC_@
T9137 TPC26T T9128 TPC26T T9132 TPC26T
C9124 0.1UF/25V vx_c0402_small 10% DSC_@
+3VS_VGA (Max:0.42A)
+1.5VO
C9125 @ 47PF/50V vx_c0402_small 5%
Q9107 DSC_@ SIR472DP-T1-GE3
VGS= 4.5V , Rdson = 15mOhm
VGS= 10V , Rdson = 12mOhm
+1.5VS_VGA_SW_R
C9121 0.033UF/16V 10% DSC_@
R9110 22KOhm vx_r0402_small 1% DSC_@
T9138 TPC26T T9134 TPC26T T9133 TPC26T
C9122 0.1UF/25V vx_c0402_small 10% DSC_@
+1.5VS_VGA (Max:4.137A)
R9116 @ 47KOhm vx_r0402_small 1%
T9125 TPC26T
+12VSUS
C9123 @ 47PF/50V vx_c0402_small 5%
T9130 TPC26T
T9126 TPC26T
Q9108 DSC_@
R9109 560KOhm vx_r0402_small 5% DSC_@
+12VS_VGA (Max:0.01A)
25,87 DGPU_PWROK
3.3V --> 1.05V --> VGA_CORE --> 1.5V
+12VSUS
R9108 560KOhm vx_r0402_small 5% DSC_@
+5VSUS
R9107 560KOhm vx_r0402_small 5% DSC_@
DGPU_EN_PWR
Q9110A UM6K1N DSC_@
Q9110B UM6K1N DSC_@
24,30,57,92 SUSB_EC#
82,83,84,85,93 SUSB#_PWR
30,57 SUSC_EC#
83,93 SUSC#_PWR
24 VGA_PWRON
87 DGPU_EN_PWR
T9122 TPC26T
SP9100@ nb_r0402_short_5mil_small
T9118 TPC26T
T9109 TPC26T
SP9101@ nb_r0402_short_5mil_small
T9116 TPC26T
T9127 TPC26T
SP9102@ nb_r0402_short_5mil_small
T9135 TPC26T
R9121 0Ohm nonDS3_@
+3VO
C9131 @ 47PF/50V vx_c0402_small 5%
Q9115 IRFML8244TRPBF DS3_@
(Max:0.15A)
+3VSUS_DS3
C9133 0.1UF/25V vx_c0402_small 10% DS3_@
C9130 0.033UF/16V vx_c0402_small 10% DS3_@
R9122 0Ohm nonDS3_@
R9119 22KOhm vx_r0402_small 1% DS3_@
+5VO
C9132 @ 47PF/50V vx_c0402_small 5%
Q9114 IRFML8244TRPBF DS3_@
(Max:0.0287A)
+5VSUS_DS3
C9134 0.1UF/25V vx_c0402_small 10% DS3_@
C9135 0.033UF/16V vx_c0402_small 10% DS3_@
R9120 22KOhm vx_r0402_small 1% DS3_@
+12VSUS
R9117 560KOhm vx_r0402_small 5% DS3_@
+5VA
R9118 560KOhm vx_r0402_small 5% DS3_@
22,30 SLP_SUS#
Q9116A UM6K1N DS3_@
Q9116B UM6K1N DS3_@
VSUS_ON POWER
R9123 0Ohm @
+5VO
C9128 @ 47PF/50V vx_c0402_small 5%
Q9112 IRFML8244TRPBF
VGS= 4.5V , Rdson = 22mOhm
VGS= 10V , Rdson = 17mOhm
+5VSUS_SW_R
C9129 @ 0.1UF/25V vx_c0402_small 10%
R9115 1KOhm vx_r0402_small 1%
T9139 TPC26T T9141 TPC26T T9140 TPC26T
C9127 0.1UF/25V vx_c0402_small 10%
+5VSUS (Max:1A)
+12VSUS
R9114 560KOhm vx_r0402_small 5%
+5VA
R9113 560KOhm vx_r0402_small 5%
30,57,81,93 VSUS_ON
Q9113B UM6K1N
Q9113A UM6K1N
<Variant Name>
PEGATRON
Title : POWER_LOAD SWITCH
Engineer: Clark Liang
Size Custom
Project Name JM50
Rev 1.0
Date: Thursday, August 23, 2012
Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON Title : POWER_PROTECT

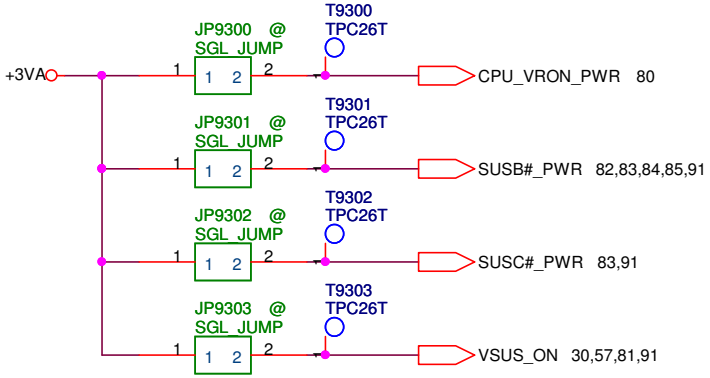
Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 92 of 94

AC_BAT_SYS	AC_BAT_SYS	45,53,81,87,88
BAT_CON	BAT_CON	60,88
+5VA	+5VA	37,60,81,91
+3VA	+3VA	6,20,26,27,30,31,57,59,60,81,88
+5VO	+5VO	52,65,80,81,82,83,85,91
+3VO	+3VO	53,81,84,85,91
+1.8VO	+1.8VO	60,84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+0.75VO	+0.75VO	83
+12VSUS	+12VSUS	28,51,81,91
+5VSUS	+5VSUS	51,57,59,91
+3VSUS	+3VSUS	4,22,24,28,30,60,81,92
+12V	+12V	60,91
+5V	+5V	57,59,60,91
+3V	+3V	24,45,57,59,61,91
+1.5V	+1.5V	5,16,17,18,57,60,83
+12VS	+12VS	28,36,48,91
+5VS	+5VS	27,36,37,48,50,51,57,80,87,91
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+1.8VS	+1.8VS	7,25,26,57,80,84
+1.5VS	+1.5VS	7,26,53,57,91
+1.05VS	+1.05VS	26,27,57,82,87
+VCCSA	+VCCSA	7,85
+0.75VS	+0.75VS	16,17,57,83
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+12VS_VGA	+12VS_VGA	60,91
+3VS_VGA	+3VS_VGA	57,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	57,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	57,70,71,72,91

FOR POWER TEST



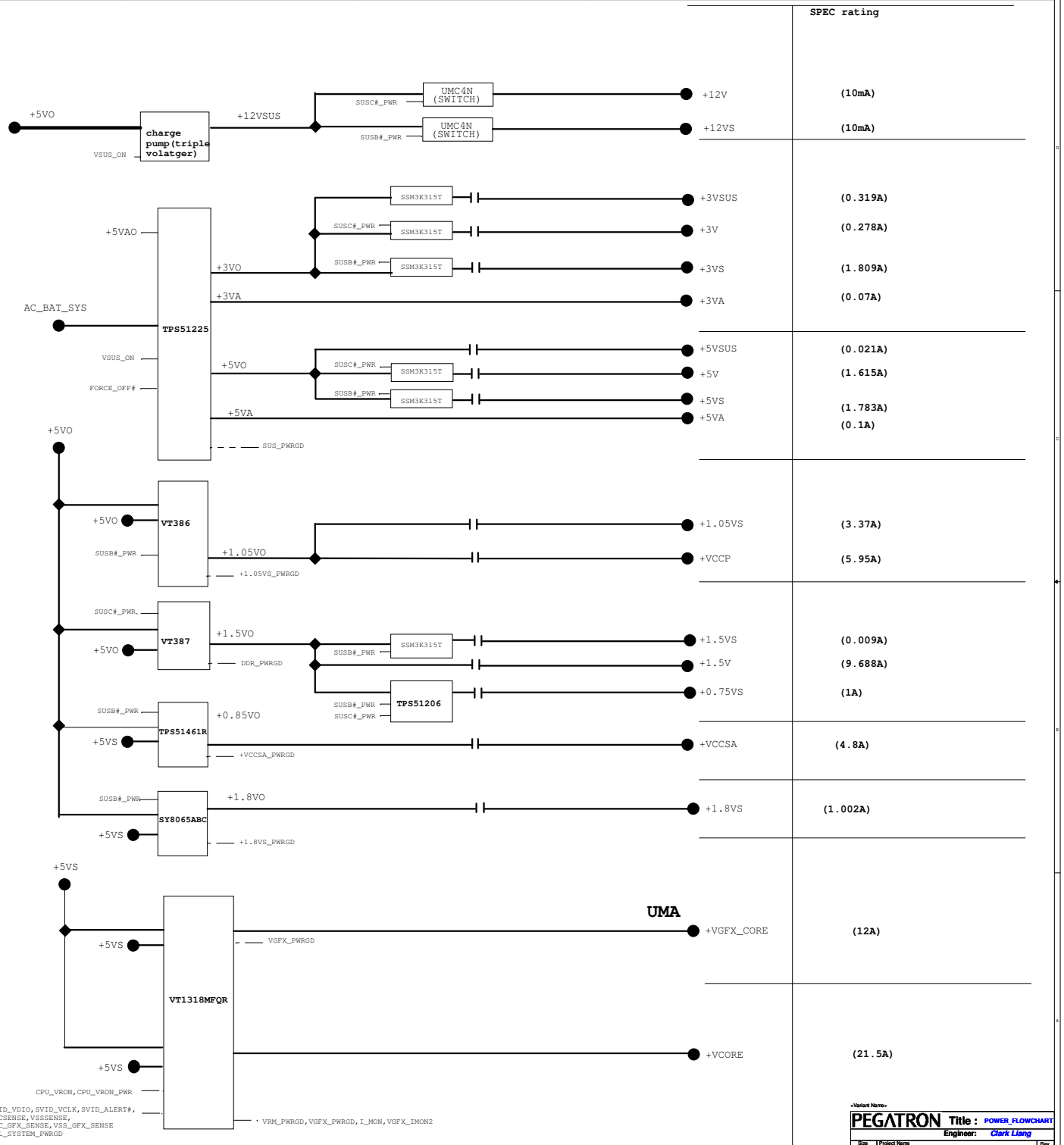
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 93 of 94



<Variant Name>

PEGATRON Title : POWER_FLOWCHART

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 84 of 94

PEGATRON	Title : ****	
BG1\HW1	Engineer: *Joyoung_Chianhg*	
Size: A	Project Name: **JM50**	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 96 of 93	

SR BOM change

SR1.1 Un-mount Q5602, Q5601 and mount R5323 and R5310

SR1.2 CE5001 un-mount

SR1.3 L3602 mount

SR1.4 R7005 un-mount

SR1.5 R7410 change 10K ohm

SR1.6 R4504 change 10K ohm for LVDS backlight

SR1.7 R7430, R7432, R7433 un-mount

SR1.8 R7608, R7611 change 162 ohm

ER

ER1.1 PI pin connect to ESD and VDD pin reserve 0.1 uF cap
ER1.2 Add diode and reserve 0 ohm for AC adapter plug in /out voice
ER1.3 U5201 change G547G1P81U for Desing IP
ER1.4 Add Card Reader LED
ER1.5 J3701, J3702, J4601, J5201, J5304,J5001 chang connector
ER1.6 R6505~R6508 change 0603 size
ER1.7 D4801 contact to 2.2K ohm for EA solution in HDMI issue
ER1.8 CPU_THERM# contact to FORCE_OFF#
ER1.9 RTC battery connector (J2001)Pin1, Pin2 swap
ER1.10 D3707, D4618, D5201, D5301, D6502, D6503, D6802 VDD pin reserve 0.1 uF cap
ER1.11 R3720 R3721 change 51ohm for consumer spec in HP
ER1.12 L4601, L4602, L4603 change 27nH and add C4622, C4623, C4624 for EA solution in CRT
ER1.13 L5301, L5302, L5306 change 0 ohm and L5305 change short pin,
C5321, C5327,C5307, C5322, C5315, C5305, C5313 change umount
ER1.14 Change R4566 from 300(0603) to 150(0402) for LVDS power sequence solution
ER1.15 USB port 0 and port 1 swap
ER1.16 Vcore_add CE8002&CE8006 to replace CE0601&CE0602
ER1.17 VGFX_CORE(IGPU) add CE8007 to replace CE0705
ER1.18 reserve M_VREF schematic
ER1.19 Reserve C2623, C2624, C4514, C4515 for WLAN solution
ER1.20 Reserve C4510, C4512, C4513 for 3G and L6002~L6004, L4502 change 47 ohm Bead
ER1.21 C6007, C6006 mount for WLAN
ER1.22 RN3002 change 2R4P
ER1.23 LED and BT schematic change to LED board
ER1.24 LED power change 5VSUS, so R5618, R5616, R5623 change 560 ohm
ER1.25 VRAM change co-lay footprint
ER1.26 Reserve C5601, C5602, C5603, C6356, C6357 to 47pF for RF request
ER1.27 Reserve C4516, C4517 to 10pF for RF request
ER1.28 U6504,U6505 change AZ3028 for EMI request
ER1.29 D6401, D6501, D6502 change ESD AZ5023 in for EMI request in LAN function
ER1.30 Add C6010 C6011 for EMI request
ER1.31 Merge Q6704 and remove U6704
ER1.32 D3720 change to mount for EMI request
ER1.34 Reserve C6913(47PF), C6902(0.1uF), C6623(47PF), C6606(22uF) for 3G
ER1.35 L6601=>0901-00HI000 FERRITE BEAD(1206)390 OHM/2A

PR

PR2.1 RTC pin define swap

PR_S01:Change C3627,C3626 from X5R to Y5V

PR_S02:According with INTEL datasheet suggest.(Power circuit mount)

PR_S03:To prevent 誤動作 PCIE Wake.

PR_S04:To change WLAN LED control by MODULE then gate control by 3G LED.

PR_S05:To change 3G LED control by MODULE.

PR_S06:To prevent leakage current and mount R for cost down.

PR_S07:RF reserve.

PR_S08:Move P.U 10K near 3G connector.

PR_S09:Change LED POWER rail from +5VSUS_LEDDB(+5VSUS) to
+5VA_LEDDB(+5VA) .(To resolve Battery LL issue)

PR_S10:Change LED POWER rail from
+5VSUS_LEDDB(+5VSUS) to +5V_LEDDB(+5V)

PR_S11:Del JP, +3VS_CR change Net name to +3VS

PR_S12:ESD change solution ,Add U6512 ,Del C6509,D6501~3,U6502,U6503,D6401

PR_S13:Change NET name to +3VS

PR_S14:Change 10uF to 22uF for wave of CRT display.

PR_S15:Add 10uF (C6803)for USB droop test.

PR_S16:D5201 PIN Swap

PR_S17:ME modify.(H6532,8,1,9,4,3,5,H6945),DEL H6944

PR_S18:EMI add.

PR_S19:Change to unmount for ME

PR_S20:RF request.

PR_S21:LED light fine-tune.

PR_S22:BIOS request for UMA and DSC platform identifying.

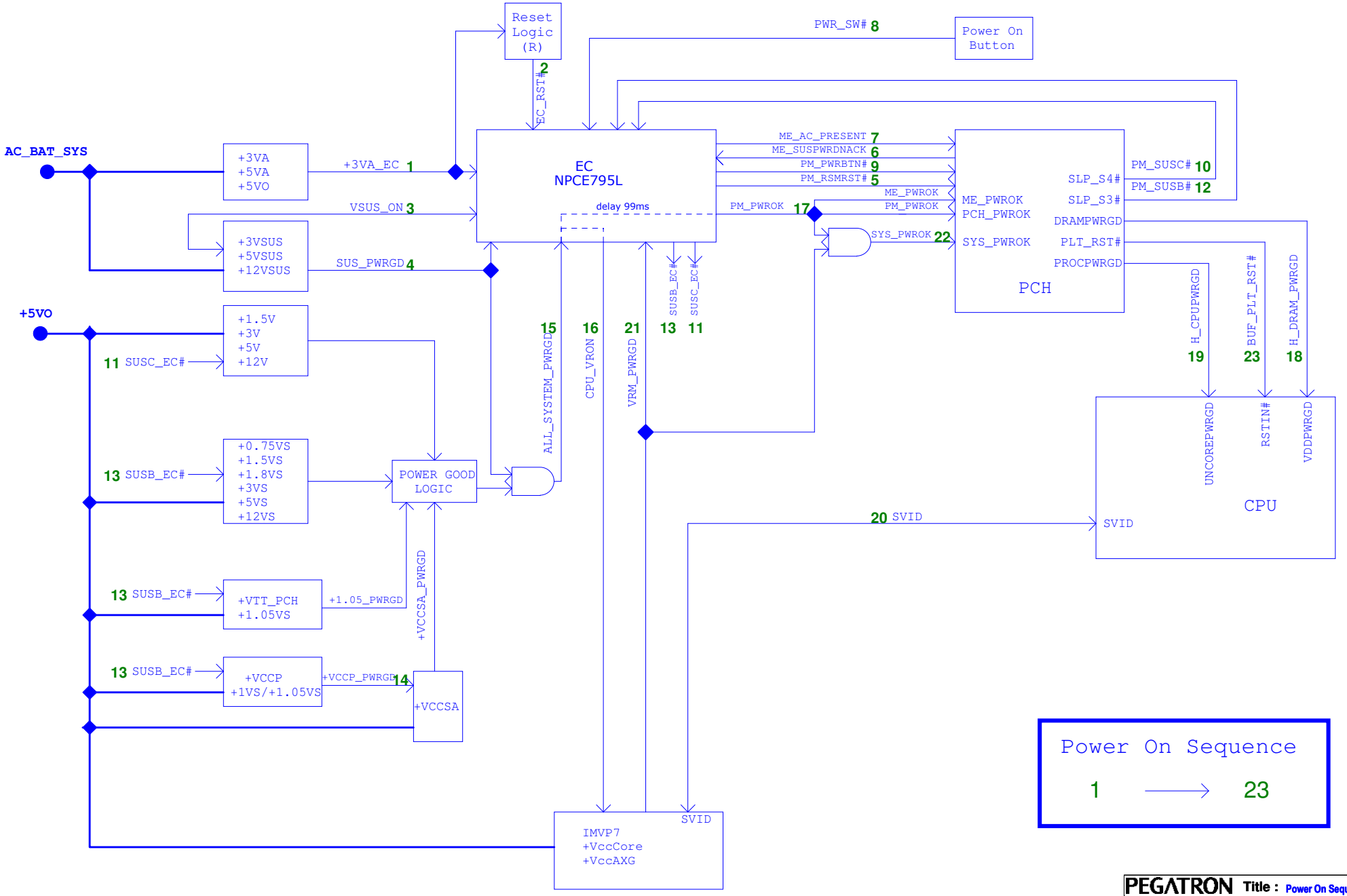
PEGATRON Title : ****

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 97 of 93

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



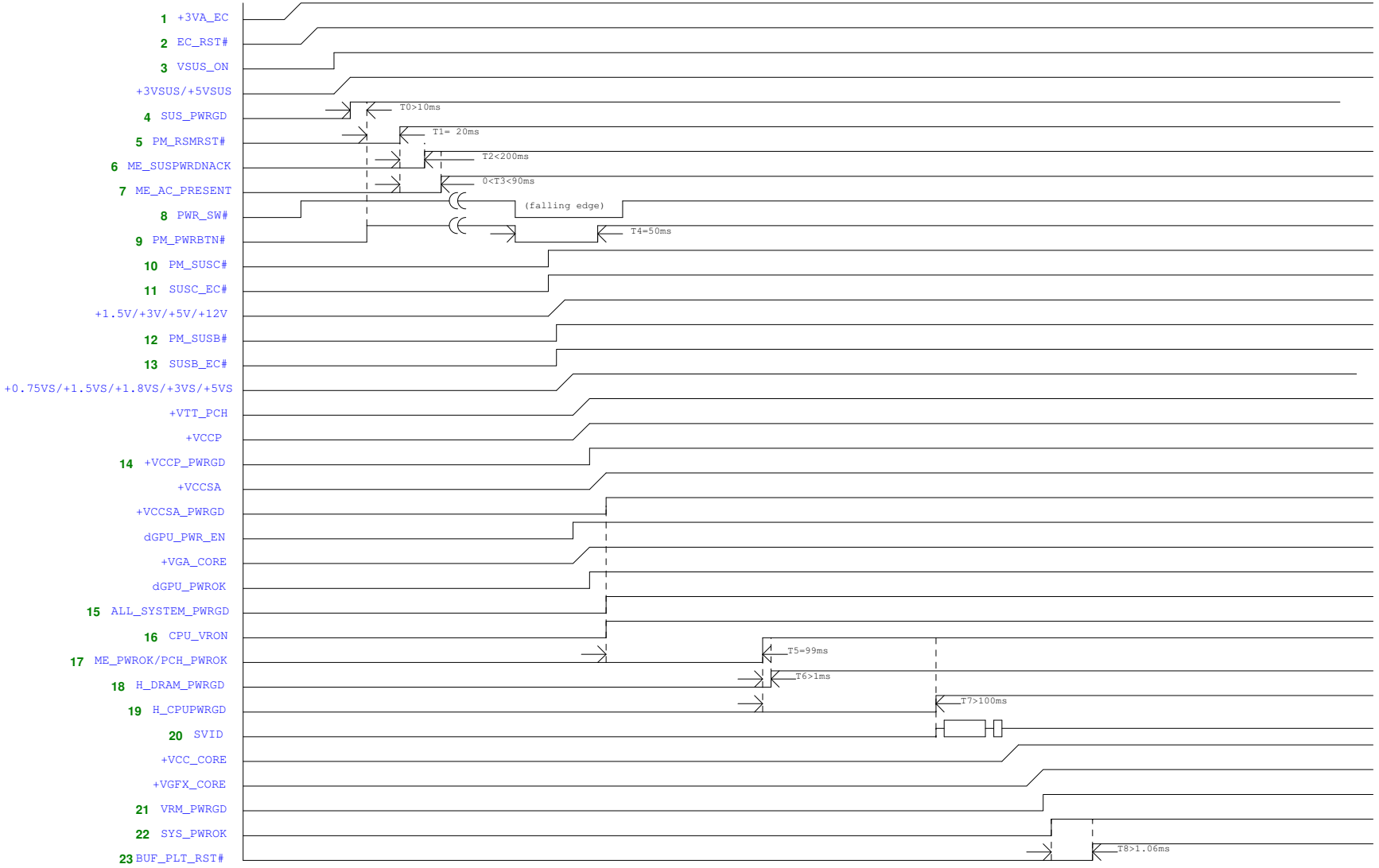
PEGATRON Title : Power On Sequence

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 98 of 93

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON	Title : Power On Timing	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 99 of 93	